NASA CR-163100

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INTEgrated Research Aircraft Control Technology with Full Authority Digital Electronic Control

F-15/F100

NASA-ED-66
TASK 12

NASA/USN/USAF

April 1980

PRATT & WHITNEY AIRCRAFT GROUP
Government Products Division
UNITED TECHNOLOGIES

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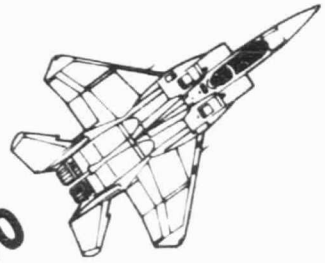

F-15/F100

NAS4-2556
TASK IV

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April 15

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UNITED TECHNOLOGIES ®

ABSTRACT

The Integrated Research Aircraft Control Technology (INTERACT) Program is a joint NASA/NAVY/USAF – sponsored activity directed toward the design and flight evaluation of advanced weapons systems of the 1980's and 1990's. The scope of this document provides baseline definitions for three major areas of the INTERACT Program:

1. *Baseline System* – This definition presents the basic hardware descriptions of the two control systems to be utilized for the test engine during the INTERACT flight test program. These systems include the Research Propulsion Control (RPC) System and the Full Authority Digital Electronic Control (FADEC) System. The definition also includes the control components which are common to the two control systems.

2. *System Requirements* – Baseline propulsion control system operational requirements defined for the INTERACT program.

3. *Development Plan* – A first tier program schedule is presented to coordinate the development of the RPC and FADEC systems in a manner which permits concurrent flight validation testing of the two systems.

This study also addresses interactions of propulsion and flight systems on an F-15 aircraft, propulsion system support equipment and test considerations leading to flight demonstration during 1983. This report, FR-11792, represents the efforts achieved under Task Force IV of NASA Contract NAS4-2556.

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ILLUSTRATIONS

TABLES

ABBREVIATIONS AND SYMBOLS

α	Angle of Attack
A/B	After burner
A/C	Aircraft
A/D	Analog to digital
AFP	Augmentor fuel pump
A/I	Anti-ice valve
AIC	Air inlet control
Aj	Exhaust nozzle area
AJR	Duct stream exhaust nozzle area request
AMP	Aircraft Management Processor
BAND	Bits per second
BIT	Built-in test
BOM	Bill of Material
CCU	Computer control unit
CENC	Convergent exhaust nozzle control
CIVV	Compressor inlet variable vane
CLB	Closed loop bench
CMOS	Complementary integrated field-effect metal oxide semiconductor
CMV	Core metering valve
CPU	Central processing unit
CPUAROM	CPU Alterable ROM
CRT	Cathrode ray tube
CTT	Cycle test time
D/A	Digital to analog
DCU	Digital computer unit
DEEC	Digital Electronic Engine Control
DFRC	NASA Dryden Flight Research Center
DMA	Direct memory access
DOS	Delivery order supplement
DPCTRAM	Dual Port cross talk RAM
EAROM	Electrically alterable Read Only memory
EHMI	Electro-hydromechanical interfaces
EHV	Electrohydraulic 4-way servo valve
EMF	Electromotive force
EMI	Electromagnetic interference
ENA	Engine noise attenuation
ENPT	Exhaust nozzle position transmitter
EPR	Engine pressure ratio
FADEC	Full authority digital electronic computer
F/B	Feedback
FET	Field effect transistor
FF_{GGH}	Gas generator fuel flow
FTIT	Fan turbine inlet temperature ($T_{T4.5}$)
FTL	Flight test letter
GFE	Government furnished equipment
GG	Gas generator
GHz	1×10^9 Hz
GND	Ground (electrical)
GSE	Ground support equipment
HPC	High pressure compressor
Hz	Frequency (Hertz)
IAR	Idle area reset
IC	Integrated circuit
IFU	Interface unit
INTERACT	Integrated Research Aircraft Control Technology
I/O	Input/output
IPCS	Integrated Propulsion Control System
kHz	1×10^3 Hz
LCF	Life cycle fatigue
LeRC	NASA Lewis Research Center
LPT	Low pressure turbine
LVDT	Linear variable differential transmitter
MB	Mega bit
MFP	Main fuel pump
MHz	1×10^6 Hz
Mn	Mach number data
Mo	Mach number clock
MOH	Maximum operating hours
MRB	Material Review Board
MV	Metering valve

ABBREVIATIONS AND SYMBOLS (Continued)

NAPC	Naval Air Propulsion Center
NASA	National Aeronautics and Space Administration
N1	Low pressure compressor speed
N2	High pressure compressor
P/C	Printed circuit
PCB	Printed circuit board
PCM	Pulse mode modulation
PROM	Programmable Read Only memory
P&D	Pressurizing and dump valve
PFRT	Preliminary flight rating test
PSR	Power supply reset
PSU	Power supply unit
P&WA/GPD	Pratt & Whitney Aircraft/ Government Products Division

P Subscripts

B	Burner pressure
FAP	Augmentor permission signal pressure
FCB	Body pressure
FGG	Gas generator fuel temperature
FMO	Backup mode hydraulic signal
FS	Servo pressure
FO	Engine main pump inlet pressure
F1	Augmentor inlet fuel pressure
F1A	Augmentor inlet fuel pressure
F1AW	Augmentor inlet fuel pressure
F2	Main pump discharge
F3AC	Augmentor metered flow discharge pressure
F3AD	Augmentor metered flow discharge pressure
F4	Gas generator control discharge pressure
RO	Free stream pressure ratio
RT	Throat pressure ratio
SO	Free stream static pressure
ST	Throat static pressure
S2	Engine static inlet pressure
TO	Free stream pressure
T2	Engine inlet pressure
T3	Low pressure compressor discharge pressure
T6	Augmentor duct pressure/LPT inlet pressure
5A1-5A5	Augmentor segment pressures

QAP	Quality Assurance Plan
QF	Quickfill
QT	Qualification test
RAM	Random access memory
RCVV	Rear compressor variable vane
R/D	Resolver to digital
RF	Rocket Fire
ROM	Ready Only memory
RPC	Research Propulsion Control
S/B	Start/Bleed valve
TAC	Tactical Air Command
T/C	Thermocouple
T/M	Torque motor
TSU	Test set unit
TTL	Transistor-Transistor Logic

T Subscripts

TO	Free stream temperature
T2	Engine inlet temperature
T2.5	Fan discharge temperature
T4.5	Fan turbine inlet temperature (FTIT)
UART	Universal asynchronous receiver-transmitter
UFC/EEC	Unified Fuel Control/Electronic Engine Control
vAC	Volts, alternating current
vdc	Volts, direct current
WOW	Weight on wheels

W Subscripts

FAC	Augmentor core fuel flow
FAD	Augmentor duct fuel flow
FGG	Gas generator fuel flow
FTOT	Total engine fuel flow

ABBREVIATIONS AND SYMBOLS (Continued)

X Subscripts

BP	Inlet bypass down position
1	Inlet 1st ramp position
4	Inlet 4th ramp position

α	Angle of attack

SECTION I
INTRODUCTION

SECTION I
INTRODUCTION

A. INTERACT WITH FADEC PROGRAM SUMMARY

INTERACT involves a joint NASA/USN/USAF effort directed at the design, development, and flight evaluation of advanced concepts in the area of control systems integration for advanced weapon systems. The broad goals of this program are:

1. Development and validation of design processes for digital integrated propulsion and airframe control systems

2. Demonstration of digital engine controls that improve performance and have the potential to improve safety and life cycle cost

3. Identification and demonstration of airplane system performance improvements identified with integrated control techniques.

To achieve these goals, the controls and avionics systems on a modern turbofan powered F-15 airplane will be modified and supplemented to provide a configuration capable of supporting the development of control technology for the 1980's and 1990's.

A significant part of the INTERACT Program will be the incorporation and flight testing of the Full Authority Digital Electronic Control (FADEC) being developed by the Naval Air Propulsion Center (NAPC). The FADEC flight test objectives include:

1. Flight environment verification of dual, engine-mounted digital control computers and demonstration of the redundant control failure accommodations

2. High-speed (1MHz) data communication between the propulsion control and other aircraft systems

3. Flight demonstration of a high-speed (1MHz) fiber optic data bus

4. Control of the aircraft inlet geometry by the FADEC computer(s)

5. Demonstration of 200 volts/meter EMI hardening capability between 10 kHz and 40 GHz

6. Flight demonstration of the latest state-of-the-art electronic technology

7. Collection of an environmental data base for development of criteria for future electronic control design and for input to current simulated mission environment test programs.

B. INTERACT WITH FADEC SYSTEM FEATURES

The INTERACT with FADEC System combines aircraft-mounted programable digital control systems with the special purpose engine-mounted control system (FADEC) to provide regulation of the engine, inlet, and flight systems on a NASA F-15 aircraft. Advanced serial digital data bus technology will be implemented to integrate the various control systems to each other and to various aircraft and ground-based data systems. Interaction with the cockpit and the aircraft central computer bus will also be incorporated. Ground facilities will be developed to support the operation of the INTERACT aircraft and the development and testing of research applications. Specifics of aircraft systems integration will be the responsibility of the INTERACT integration contractor.

The flexibility and versatility of the INTERACT flight research facility provides the opportunity to investigate a wide range of research areas related to the specific INTERACT objectives. Candidates for flight research related to propulsion and integrated control are:

- Concepts
  1. Advanced control redundancy techniques
  2. Fail-operational software
  3. Self-optimizing controls
  4. Flight path management, including:
     - Terrain following
     - Collision avoidance
     - Noise abatement
     - Optimum maneuvers
     - Energy management
  5. Self-trimming engine control
  6. Multivariable control
  7. High-speed (1 MHz) communications via optic data link between dual redundant FADEC's and between each FADEC and aircraft converter
  8. Data exchange via uplink and downlink system.
- Components
  1. Fiber optic sensors and interfaces
  2. Advanced solid state sensors and actuators
  3. Digital propulsion control components

4. Advanced fuel system components (prime reliable pumps, simplified fuel management hardware)

5. Cockpit displays

6. MIL-STD-1553 data bus

C. PROGRAM STRUCTURE

The INTERACT with FADEC Program is divided into three phases: Phase I (Preliminary Design) will develop the requirements, systems configuration, and approach necessary to meet the program goals and objectives. Phase II (Final Design and Development) will provide and perform initial testing on the aircraft, ground support, and FADEC systems. Phase III will include flight testing of the FADEC and integrated controls. The aircraft will then be available for on-going research in advanced control concepts and components. An airframe integration contractor, selected by NASA, will be responsible for carrying out the objectives of the INTERACT Program.

NASA Dryden Flight Research Center (DFRC) will have overall project management for the aircraft and ground support systems development required for flight testing of the FADEC and integrated controls. DFRC will also conduct the flight tests. NAPC will manage the FADEC Program and support the FADEC flight tests. NASA Lewis Research Center (LeRC) will provide technical assistance and coordination to both DFRC and NAPC efforts.

A Propulsion Control System configuration capable of supporting the specific NAPC flight test objectives and the INTERACT program goals will require an integration of engineering and hardware responsibilities. Requirements for NASA support of the planned FADEC program are defined below:

1. A Bill-of-Material F100 engine and all support requirements for sea leve level and altitude engine testing, except for the Controls Engineering coverage required for "FADEC Specific" testing.

2. Two (2) sets of electro-hydromechanical interfaces (EHMI), control system plumbing, brackets, and support equipment. This procurement is covered under NASA contract NAS4-2670.

3. The design and procurement of a bulkhead connector panel and the installation of this panel on the F100 engine. The panel acts as a common interface point for all electrical cabling interconnecting the FADEC control system with the aircraft.

4. The design, installation, and procurement of the electrical cables required to interface the aircraft with the EHMI, sensors, and other control system components.

5. An aircraft mounted converter box that will convert the optic signals transmitted between the aircraft and the FADEC controls, into an electrical format compatible with the aircraft data bus structure. The converter box will allow the FADEC system to act as a remote terminal on the aircraft data bus.

6. Modification of the aircraft Air Inlet Control (AIC-12) ad determined necessary to interface the AIC-12 with the FADEC control system.

7. Installation of the dual FADEC control system on the F100 engine, including the engine case modifications necessary to accommodate the dual FADEC system.

8. The cockpit interface providing the pilot the ability to demonstrate the dual computer fault accommodation logic.

D. SCOPE

The scope of this document provides baseline definitions for three major areas of the INTERACT with FADEC Program:

1. Baseline System -- This definition presents the basic hardware descriptions of the two control systems to be utilized for the test engine during the INTERACT flight test program. These systems include the Research Propulsion Control (RPC) System and the Full Authority Digital Electronic Control (FADEC) System. The definition also includes the control components which are common to the two control systems.

2. System Requirements -- Baseline propulsion control system operational requirements defined for the INTERACT program.

3. Development Plan -- A first tier program schedule presented to coordinate the development of the RPC and FADEC systems in a manner which permits concurrent flight validation testing of the two systems.

The material presented in this document provides the baseline data required to permit the INTERACT with FADEC program to be implemented. Implementation of the program will be accomplished through multiple NASA and NAPC contracts to several aerospace companies. Extensive coordination will be required between these companies, NASA, and NAPC to expand the presented baseline data to the depth of detail necessary for successful demonstration of the program goals.

SECTION II
INTERACT PROPULSION CONTROL BASELINE SYSTEM

SECTION II
INTERACT PROPULSION CONTROL BASELINE SYSTEM

A. OVERVIEW

The INTERACT with FADEC propulsion control system baseline configuration consists of three major sections: the Full Authority Digital Electronic Control (FADEC) computers, the Research Propulsion Control (RPC), and the Electro-Hydromechanical Interfaces (EHMI). The RPC and EHMI combine to provide a control system with the flexibility necessary to meet the overall goals of the INTERACT program. The FADEC computers and EHMI combine to provide the control system that will achieve the specific Navy flight test objectives. Conversion from one control system to another can be accomplished by changing interface cables within the aircraft. Figure II-1 shows the anticipated aircraft arrangement for the INTERACT Propulsion Control System elements.

B. FADEC CONTROL SYSTEM

Figure II-2 shows the flight configuration of the FADEC control system. Two interchangeable FADEC controls and associated sensors, with optic data transmission between the two units, will be incorporated to provide fail operational control system capability. The FADEC controls will also interface with systems within the aircraft via the aircraft data bus structure. This interface will accommodate required data transmission, cockpit interaction, and control of the aircraft inlet geometry from the FADEC computers. Commands to the EHMI will provide all functions required for control of the F100 engine. A detailed description of the FADEC System is presented in Section VI.

C. RESEARCH PROPULSION CONTROL

Figure II-3 illustrates the RPC Flight configuration. The Honeywell HDC-601 control system used in the Air Force IPCS program will be adapted for use as the RPC with full authority control over the F100 engine by way of commands to the EHMI. The RPC will also interface with the aircraft Data Bus system and with the same sensor complement used in the FADEC System (a dedicated pressure sensor box will be required for the RPC system). Section VII presents a more detailed discussion of the RPC system.

D. ELECTRO-HYDROMECHANICAL INTERFACES

The EHMI will provide actuation interfaces with the engine fuel flows, the compressor and nozzle variable geometries, and the ignition systems. The engine generator, augmentor pump controller, and electrical cables are considered part of the EHMI. The rest of the engine control components are bill-of-material (BOM) for the F100. The EHMI will also provide a backup hydromechanical gas generator control for use in the event of second level electronic control failure. The EHMI are described in detail in Section V.

E. ELECTRO/OPTIC INTERFACES

A cost-effective approach for interconnecting the components of the INTERACT with FADEC Propulsion Control System has been conceived. A bulkhead connector panel on the fan case of the F100 engine will serve as the termination point for all propulsion system-related functions. Switching from the FADEC to the RPC system will only require connector hookup changes at the bulkhead panel. Specific cabling requirements are described in Section IV, F100 Engine Update Requirements.

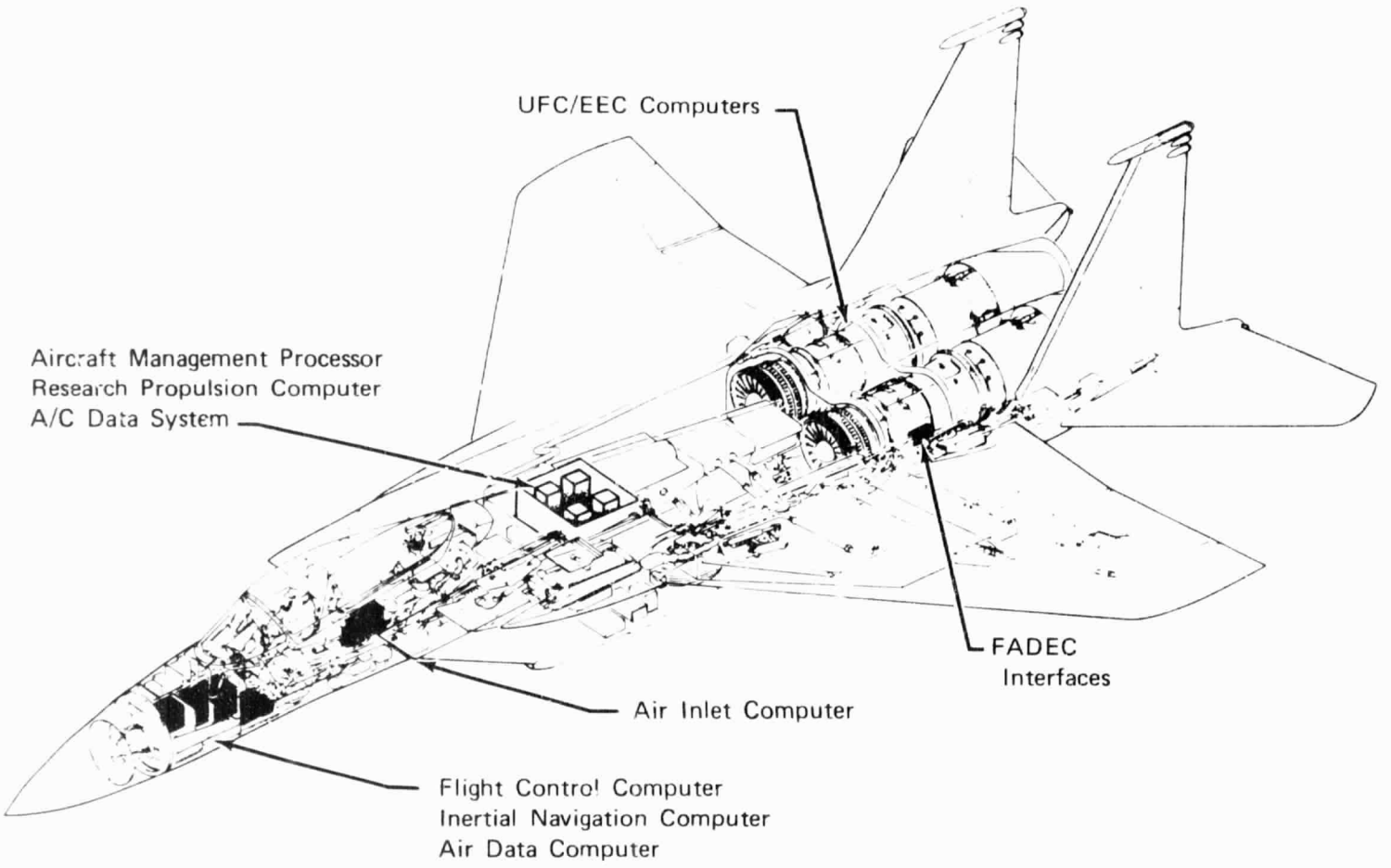

Figure II-1. INTERACT Aircraft Arrangement

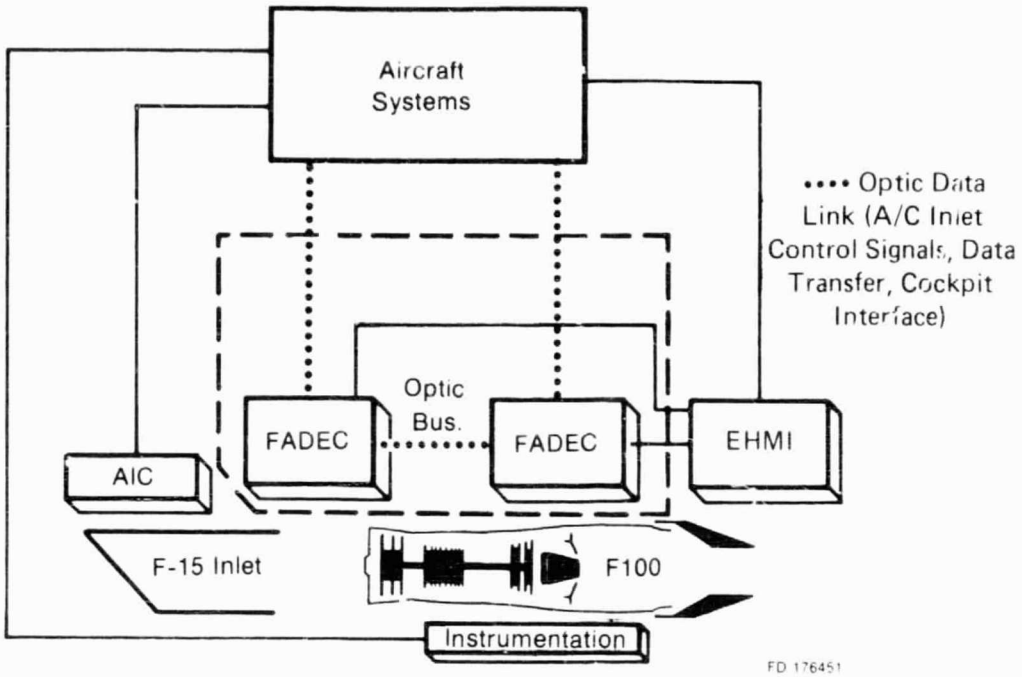

Figure II-2. INTERACT with FADEC

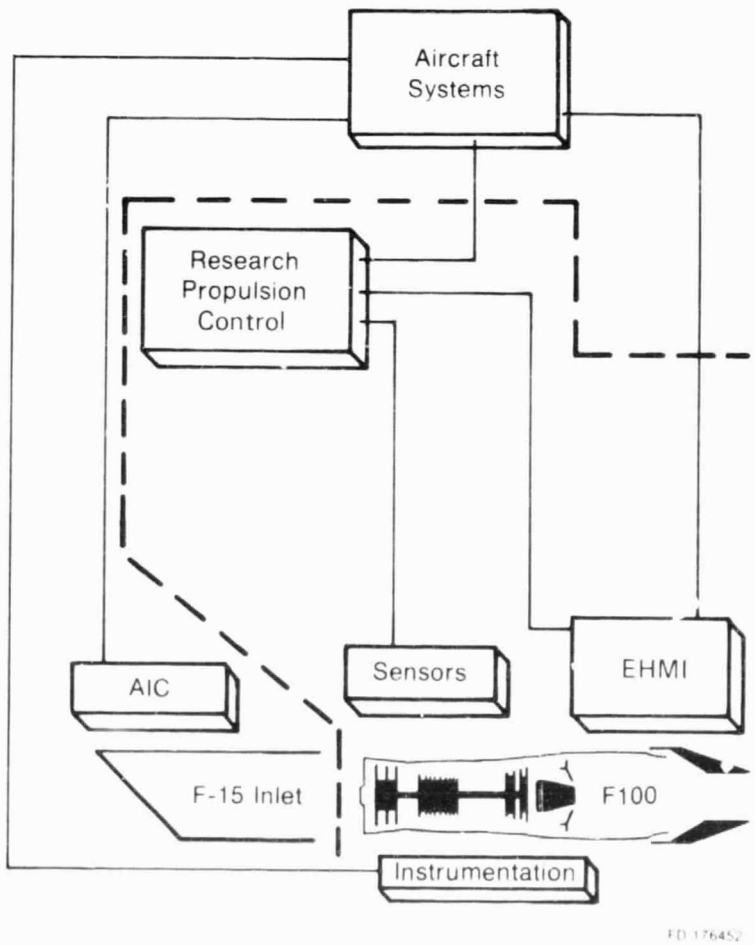

Figure II-3. INTERACT with RPC

SECTION III
OPERATIONAL REQUIREMENTS AND SOFTWARE MANAGEMENT

SECTION III
OPERATIONAL REQUIREMENTS AND SOFTWARE MANAGEMENT

This section provides a preliminary definition of propulsion system operational requirements and management of related software generated during the INTERACT with FADEC program. It is understood, however, that overall operational requirements will be coordinated through the INTERACT Integration Contractor.

A. PROPULSION SYSTEM OPERATIONAL REQUIREMENTS

1. Hardware that will be used in the flight test program must be qualified for flight in accordance with requirements coordinated with DFRC (reference Dryden Process Specification 21-2).

2. The FADEC engine-mounted system will have complete control of the engine from start to full augmentation. No single malfunction within a FADEC control shall cause both controls to become inoperable.

3. The RPC control will have full control of the engine from start to full augmentation when the RPC system provides the active control.

4. A hydromechanical gas generator control is included in the EHMI that is capable of providing safe operation of the test engine in the event the digital electronics become inoperable.

B. COMPONENT FAILURE ACCOMMODATION

Hardware failure accommodation incorporated in the EHMI components ensures safe engine operation in case of a system malfunction. Typical failure accommodation results from:

- Loss of Electrical Power

  1. The second stage of the electrohydraulic servo valves in the gas generator control is null biased so that the actuators will slew in a predetermined direction to a safe output position. For example, fuel flow slews to minimum flow, RCVV's to full-cambered position, exhaust nozzle area to full closed, etc.

  2. The hydromechanical backup control system is armed when the backup mode solenoid loses electrical power.

  3. Augmentor operation is inhibited.

- Loss of Signals to the Backup Control

The back-up control fuel flow and RCVV schedules will slew to fail-safe plateaus if malfunctions in the sensing systems occur.

- Loss of Sensor Signals

  Redundant sensors are incorporated for the critical parameter calculations, such as N1, T_{T2}, and FTIT. Loss of critical pressure inputs can be accomplished by parameter synthesis logic programmed in FADEC.

C. DATA SYSTEM DOWNLINK

The INTERACT program, illustrated in figure III-1, will probably utilize the downlink system. The estimated data sampling rate of the propulsion system will be 20 samples per second. It is anticipated that the propulsion system will utilize 256 of the 512 MIL-1553B data bus words available. Engine instrumentation and selected FADEC data going directly to the A/C data systems will consist of approximately 100 additional words.

D. SOFTWARE MANAGEMENT AND CONTROL

The NASA DFRC Software Control Management Policy (DFRCI 8100) requires that software control procedures be adequate to satisfy the established software management level:

Level A. Software failure could cause loss of life or limb, compromise public safety, or result in substantial financial loss

Level B. Software failure could cause mission failure

Level C. Software failure could cause inaccurate results or inefficient use of resources.

All software in the FADEC and RPC programs have been established as "Level B," and the software management will be structured accordingly. Anticipated software relationships in the INTERACT with FADEC program are shown in table III-1.

Table III-1 Engine/Aircraft Software Relationship

FADEC	*RPC*	*AMP*
Propulsion Control	Propulsion Control	Inlet Control
Redundancy Management	Self Test	Flt Control Interface
Self Test		Auto Throttle Interface
Inlet Control		Self Test
		Uplink
		MIL 1553B Primary Control
		Air Data Interface
		Downlink Data Interface

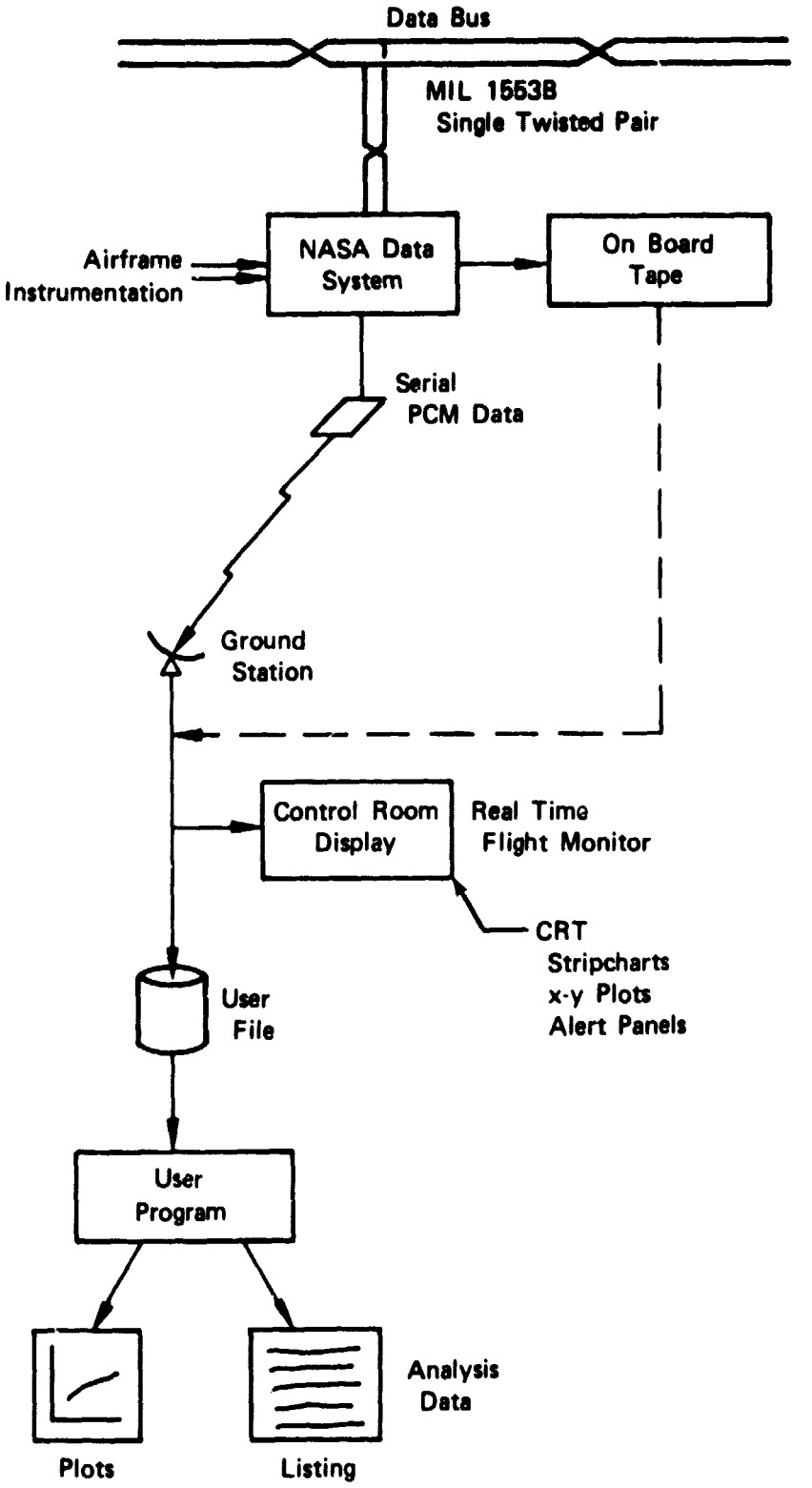

Figure III-1. INTERACT Flight Support Data System

1. Software Design and Development at P&WA

The initial design of all software will be reviewed with NASA to assure that goals of the research software can be met by the structure to be implemented. The final design will then be documented in a design workbook detailing the philosophies leading to the implementation and will cover all modifications to that original concept as the structure evolves. This document will include descriptions of interface hardware functionality, processor constraints, and functional requirements.

During the implementation and debugging phase, all modules will be subject to a functional test representing realistic operating conditions that the system will encounter. Results of these tests will become a part of the software workbook. Prior to making this software available for system test, a complete functional verification plan will be provided to NASA and will be conducted on the software package.

2. Software Configuration Control at P&WA

All RPC and FADEC software will come under configuration control when it is released after completion of the breadboard system integration tests at P&WA. From this time on the software will be controlled by the P&WA software configuration management process which requires each released assembly to be identified by a unique number. This system requires that a software description document be published defining the structure and design philosophy of the item. The basis for this document will be in the workbook maintained during the design phase. This system also provides for protected storage of the source code such that any copies that are required for use or documentation are assured to be identical.

Each identified release of software will be subject to a functional verification test representing realistic operating conditions. This test plan will be available for review by NASA. The final output of the simulation tests will be a fresh release of the software and its associated documentation.

Program modifications made between releases will be made by machine code patches such that high confidence exists that a majority of the software is unchanged and that verification emphasis can be placed upon the changes themselves. These changes will be documented by software change notices which include the actual changes made and source documentation which can be included with the original assembly source. This between-release change will be designated in the loadable program as a change number to the identification number assigned at time of original release. Each of these modifications will be subject to verification via the functional tests performed on the original release (as modified to reflect the change).

3. Software Control At NASA LeRC

After the F100 engine and controls (FADEC and RPC) are delivered to NASA, the software control procedures will be identical to those established in paragraph 2, with the exception that the NASA Software Manager or his designate will participate in approval of all software changes.

4. Software Control At Dryden

All released software will be subject to P&WA controls identical to those described above. In addition, the documentation for the first pre-flight release will be brought up to date to include all revisions and the design document will be restructured to reflect a software workbook to document all program change requests and program change notices. This document will also contain complete descriptions of the hardware configurations covered by the software, and the design philosophy.

Released software will be subject to review by NASA, as will all changes proposed and implemented. Many research module changes will be implemented in the form of machine code patches. This is an effective method of isolating the changes such that verification emphasis can be placed on the new elements and a limited amount of time placed on backtracking old software. Changes which can be so implemented will be documented by software change notices and reviewed by NASA. In addition, source notations will be produced to be filed with the source listing relating to the modified module. The modified software will be tested by the functional tests previously approved for the release (modified as required). If the revision is judged to be too significant to be effectively implemented in patch form, a new release of the software will be required and the function validation test will be modified and the software documentation will be revised to reflect the new release.

Specific software support from NASA-Dryden necessary for the FADEC flight test program will be coordinated during the development of an INTERACT with FADEC flight test plan.

SECTION IV
F100 ENGINE UPDATE REQUIREMENTS

SECTION IV
F100 ENGINE UPDATE REQUIREMENTS

Government furnished equipment (GFE) engines will require modification by P&WA to a configuration that will provide the operational life requirements of the INTERACT program and accept the new control system components. Engine gas path modifications will be made only to the extent necessary to insure adequate engine life exists for the projected INTERACT flight program. Engine case modifications will be similar to those already substantiated in previous engine development programs and only as required to mount the INTERACT control components.

The extended INTERACT engine program requirements have been identified to include:

1. 200 flight hours

   A minimum of 60 hr of operation at sea level and altitude testing prior to flight test

2. 1200 TAC LCF cycles are estimated to be accumulated in 200 hr of INTERACT test activity.

Service life of engine rotating hardware is limited to specific maximum operating hours (MOH) or TAC cycles (LCF cycles), whichever occurs first, before overhaul or disassembly/inspection is required. Engine parts life limits are defined in the F100 Service Manual TO 3-666 and MCN TO 6-969.

A. INTERACT/F-15 ENGINE

The GFE engines to be used as propulsion vehicles in INTERACT are P680059 and P680093, originally built for the F-15 flight test program for the purpose of evaluating an Improved Stability Fan having a reduced span (bulged inner diameter) flow path. These two engines, designated F100-PW-100(2 7/8), are identical to the F100(2) except for the improved stability fan. The engines also incorporate flight instrumentation capability. They remained in the F-15 flight test program until the early part of 1976 at which time the two engines were transferred to NASA in support of their F15 Flight Research Program. The engines were sent to the Propulsion Systems Laboratory at the NASA LeRC for flow calibration and later returned to NASA DFRC for the Flight Research Program to evaluate:

1. Engine/inlet compatibility of F15 and F100 engine
2. Inlet integration
3. Nozzle/boattail integration
4. In-flight thrust measurements.

Both engines presently have approximately 400 total engine operating hours and will be due for overhaul in the near future.

1. Engine Update Plan

In determining the extent of update required for engines P680059 and P680063, a complete structural analysis was made by P&WA on engine P059 based on its history received from NASA DFRC. This hardware analysis became a major factor in determining the engine use criteria for the INTERACT program.

Existing hardware usability based on the INTERACT extended life requirement was the basis of all the following criteria items: A 200-flight hour INTERACT testing requirement and a 60-hr PFRT test, plus current NASA testing and past engine history, were combined to evaluate the extent of hardware update or replacement required.

Past engine history was reviewed to determine the extent of any Engineering Changes, Service Bulletins, and/or Service Test Letters which had been incorporated in the engines during past overhauls and would be required for the projected INTERACT duty cycle.

A review of all life-limited and LCF parts was made in accordance with F100 service manuals. Estimated TAC cycle determinations included the effects of small and large amplitude thermal cycles on engine life. Equivalent LCF cycles of engine modules, parts, and components were estimated based on F100 (3) operational experience. This procedure was used to determine the accumulated TAC cycles that would be used during the extended life of 200 additional flight hours.

Major durability changes incorporated in F100(3) engine, based on F100(2) experience, were included in the update, such as the removal of titanium parts in the HPC, to increase the overall life and safety of the engine/vehicle.

B. INSTALLATION OF REDUNDANT FADEC COMPUTER ON THE F100 ENGINE

Installation of the second FADEC computer on the F100 engine requires limited rearrangement of existing components, plumbing, and electrical cabling. Figure IV-1 shows a preliminary mounting location for the second computer in the area of the main ignition exciter. This approach is believed to have minimal impact on the F100 installation envelope.

C. SYSTEM INSTRUMENTATION

Requirements exist during the flight test evaluation of the INTERACT system to measure and evaluate a significant quantity of propulsion system related parameters. These parameters may be grouped into four major categories: pressure (pneumatic and hydraulic), temperature, vibration, and other signals (speed, flow, digital data, etc.).

The instrumentation requirements will depend heavily on the type of test being performed and will require coordination with the integration contractor.

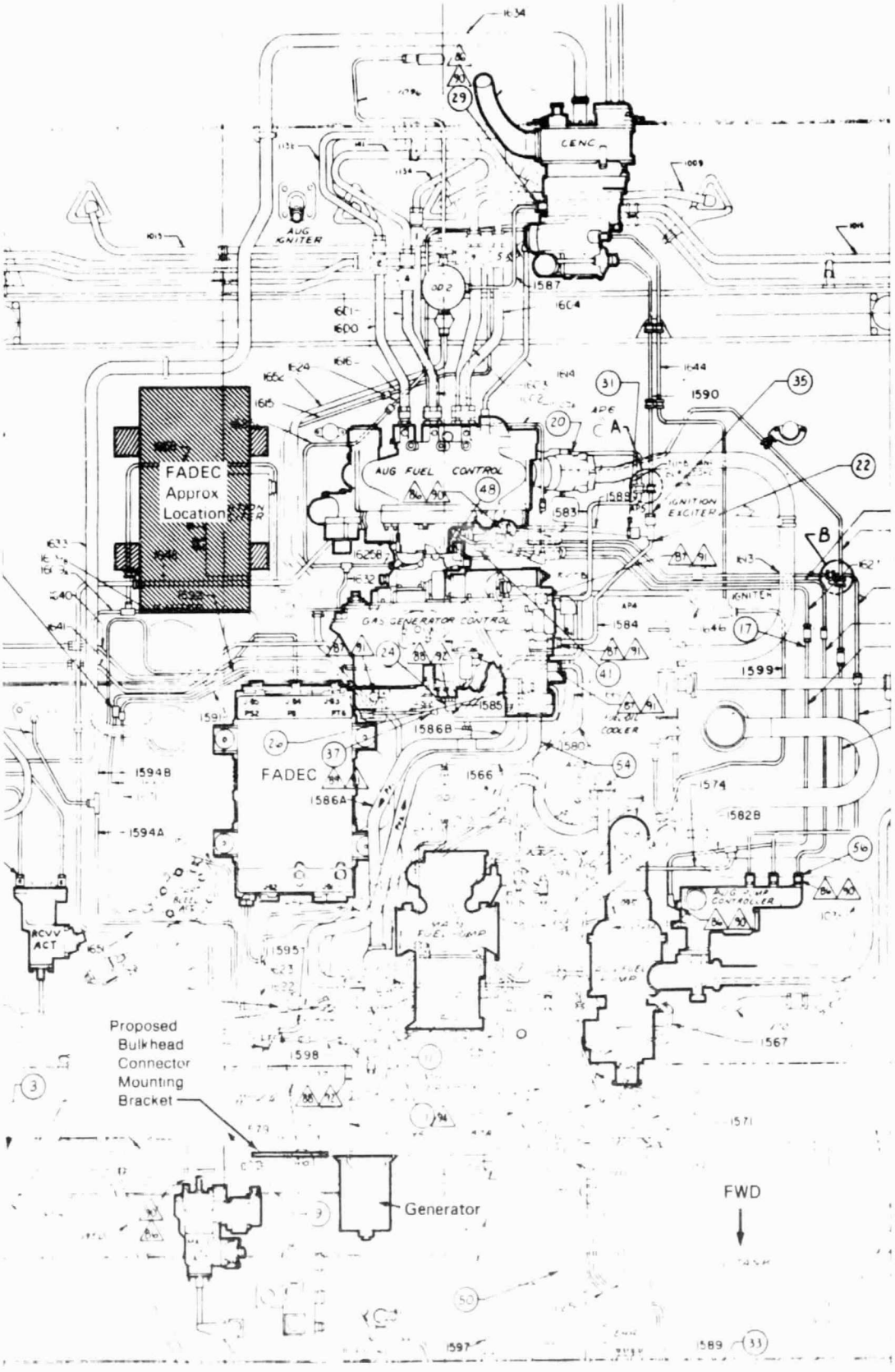

Figure IV-1. FADEC Secondary Approximate Mounting Location

1. Current Engine Instrumentation

The engines designated for the flight test program include instrumentation and rakes that provide access to a variety of engine parameters, such as those shown in figures IV-2 and IV-3. Requirements for additional instrumentation will be coordinated with the integration contractor during initial stages of the program.

2. Control Component Instrumentation

Provisions should be made to measure a variety of control system parameters for the purpose of special test requirements or system troubleshooting. Table IV-1 shows a preliminary list of the required control system parameters.

3. Engine Performance Instrumentation Kits

P&WA provides special engine instrumenation kits which allow accurate measurement of selected parameters. These kits can provide additional diagnostic data for flight test evaluation.

D. ELECTRO-OPTICAL INTERFACES (CABLING)

1. FADEC System Cabling

The FADEC engine-mounted primary and secondary control systems will be electrically wired to the EHMI and airframe as shown in figure IV-4. The bulkhead connector mounting panel acts as a common distribution point for all engine signals and power. Figure IV-1 shows the proposed location of this panel.

Optic links will be used to fill two requirements in this system. An optical data link will provide information transfer between the two engine-mounted FADEC units, and each control will be tied to the aircraft data system via a converter box (see section VI-4). The serial digital data transmitted between the primary and secondary controls will consist of both engine sensor information and health status. The serial digital data transmitted between the FADEC computers and the aircraft systems, will consist of sensor information, health status, descrete signals to the cockpit, and communication with the aircraft air inlet control.

2. RPC Cabling

The cabling requirements from the RPC to the engine sensors and EHMI will also be accomplished at the bulkhead connector panel. The changeover from the two FADEC units to the RPC will require removal of the FADEC connectors and insertion of the RPC connectors on this panel, as shown in figure IV-4.

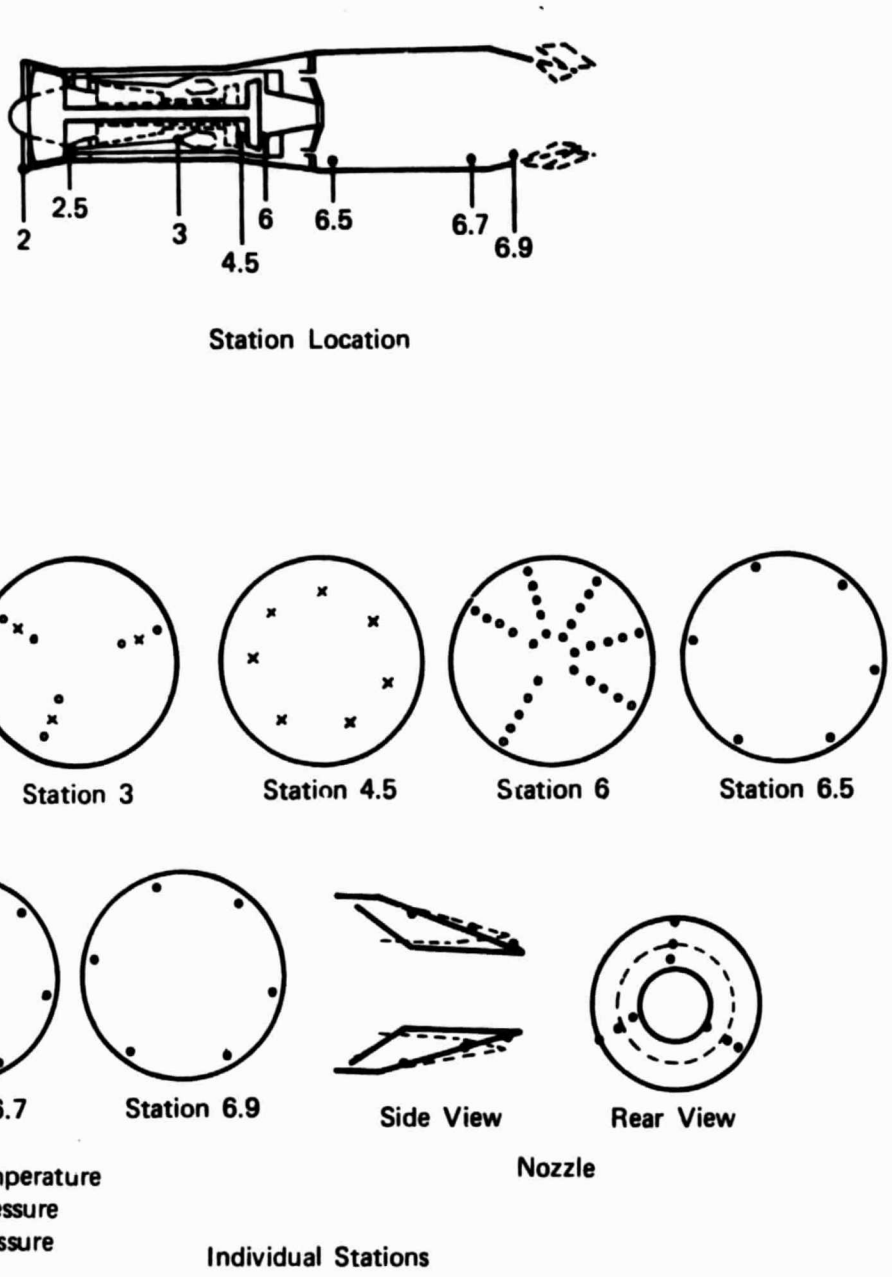

Figure IV-2. F100 Individual Station Instrumentation

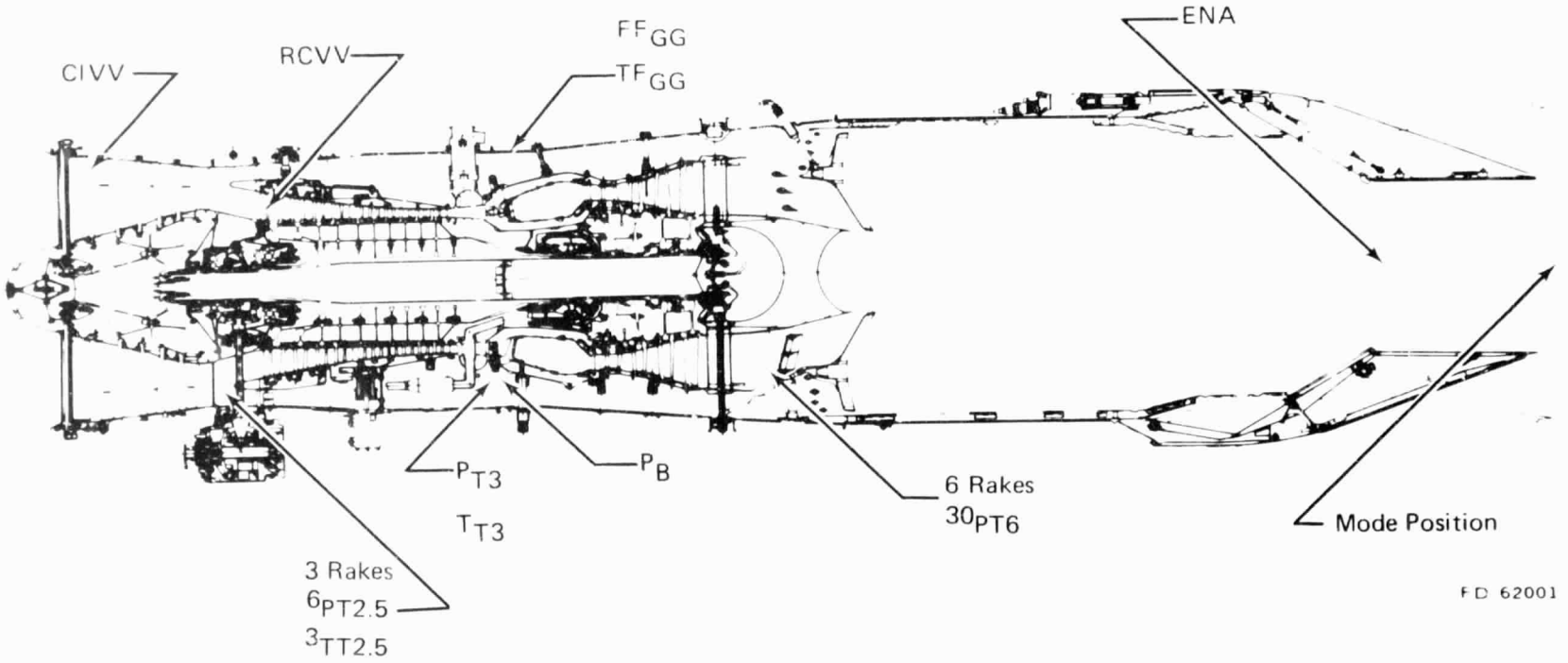

Figure IV-3. P059/P063 Instrumentation

Table IV-1. Preliminary Control Component Instrumentation Requirements

Pressures

P_{T2}	P_{F1}	P_{FMO}
P_{S2}	P_{F2}	P_{F5A1} thru P_{F5A5}
P_{T6}	P_{F4}	Others
P_{T3} (P_B)	P_{F1A}	
P_{FO}	P_{FAP}	

Temperatures (Chromel-Acumel T/C's)

T_{T2}	FTIT
$T_{T2.5C}$	TFGG
$T_{T2.5H}$	

Speeds

N_1
N_2

Flows

W_{FTOT}
W_{FGG}

Variable Geometry

RCVV
CIVV
Anti-Ice Valve
AJR (Cenc Resolver)
Start Bleeds

Cockpit

PLA
Mode Solenoid Position

Others

- Mo
- Component Environment Pressures and Temperatures
- Ignition Pulses

Vibrations

FADEC – Internal, Case and Mount Brackets

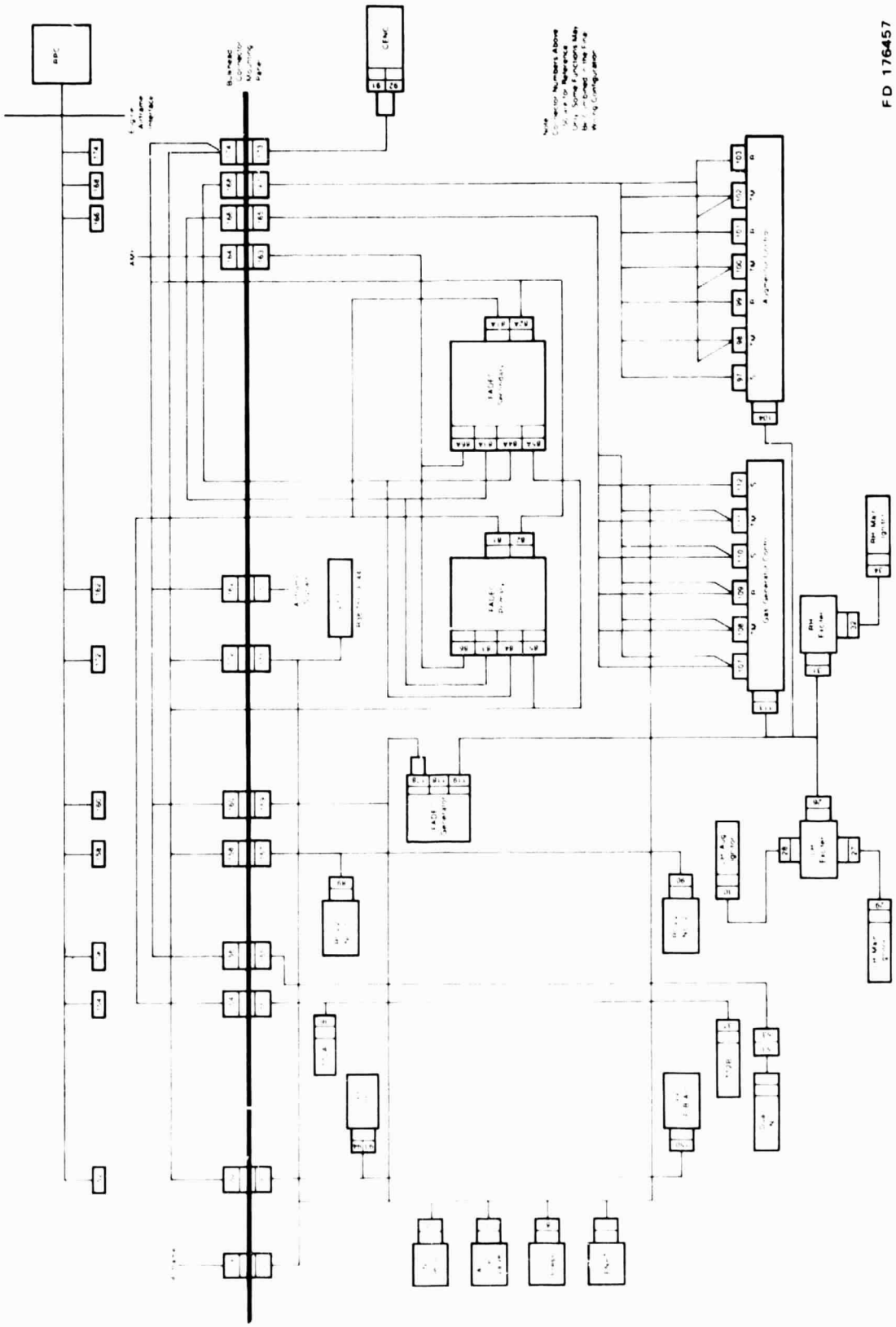

Figure IV-4. FADEC Primary and Secondary Systems Electrical Schematic

3. Cable Definition

The cables required to interface the FADEC and RPC computers with the EHMI's must be capable of carrying the following signals:

- Torque motor requests
- Resolver feedbacks
- Discretes (solenoids, switch closures)
- Sensor information
- Electrical power
- Ignition
- Airframe signals
- Air Inlet Control

The overall cable system dimensions, electrical connectors, and wiring diagrams will be coordinated with the integration contractor. All cables shall be of flexible construction, consisting of a metallic outer sheath enclosing twisted, shielded conductors and insulation. The cables will meet the same design criteria (AFSC design handbook 1-4) required for current F100 engine cables.

E. INTERACT/FADEC QUALITY ASSURANCE PLAN FOR INTERACT PROPULSION SYSTEM

1. Scope

This plan describes INTERACT/FADEC Quality Assurance Plan (QAP), shown in figures IV-5 and IV-6, to be used in the acquisition and flight testing of the Interact F100 engines. Provisions of this document are in addition to the requirements contained in the following documents:

MIL-C-45662A – Calibration System Requirements

MIL-STD-1520 – Corrective Action and Disposition System for Nonconforming Material

MIL-STD-1535 – Definition Appendix

2. Quality Program Management

The Quality Program shall be administered through the F100 Quality Assurance Manager. The Quality Program at P&WA/GPD for parts and assemblies procurement, fabrication, and assembly and test operations is controlled by: (1) Quality Engineering, (2) Quality Assurance, and (3) Quality Review groups reporting to the Quality Control Manager. These groups maintain responsibility for (1) method planning, gage procurement, and control; (2) product verification; and (3) disposition of nonconforming materials and corrective actions, respectively. Laboratory release of incoming material is controlled by the Materials Control Laboratory.

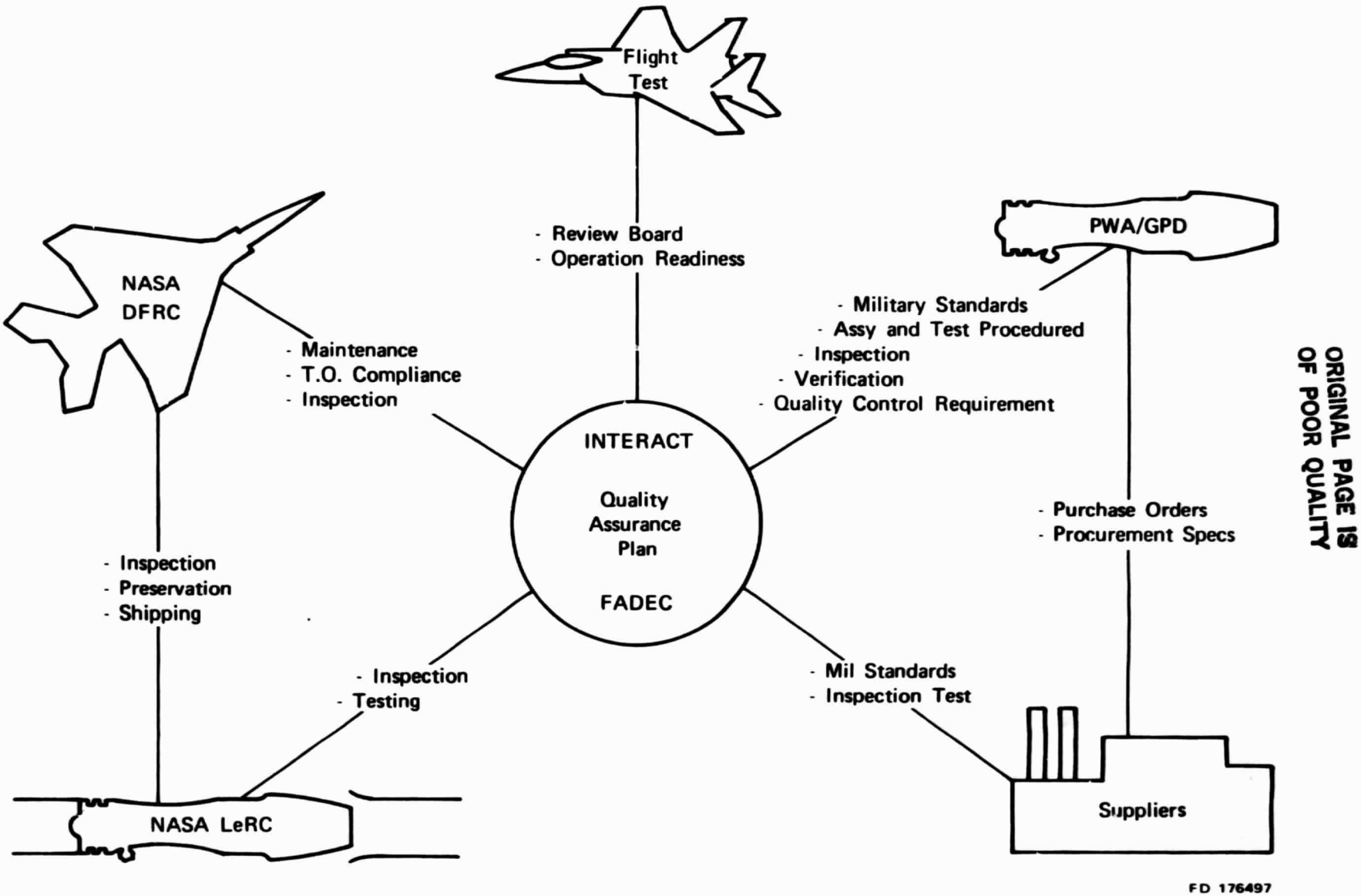

Figure IV-5. INTERACT Quality Assurance Plan Overview

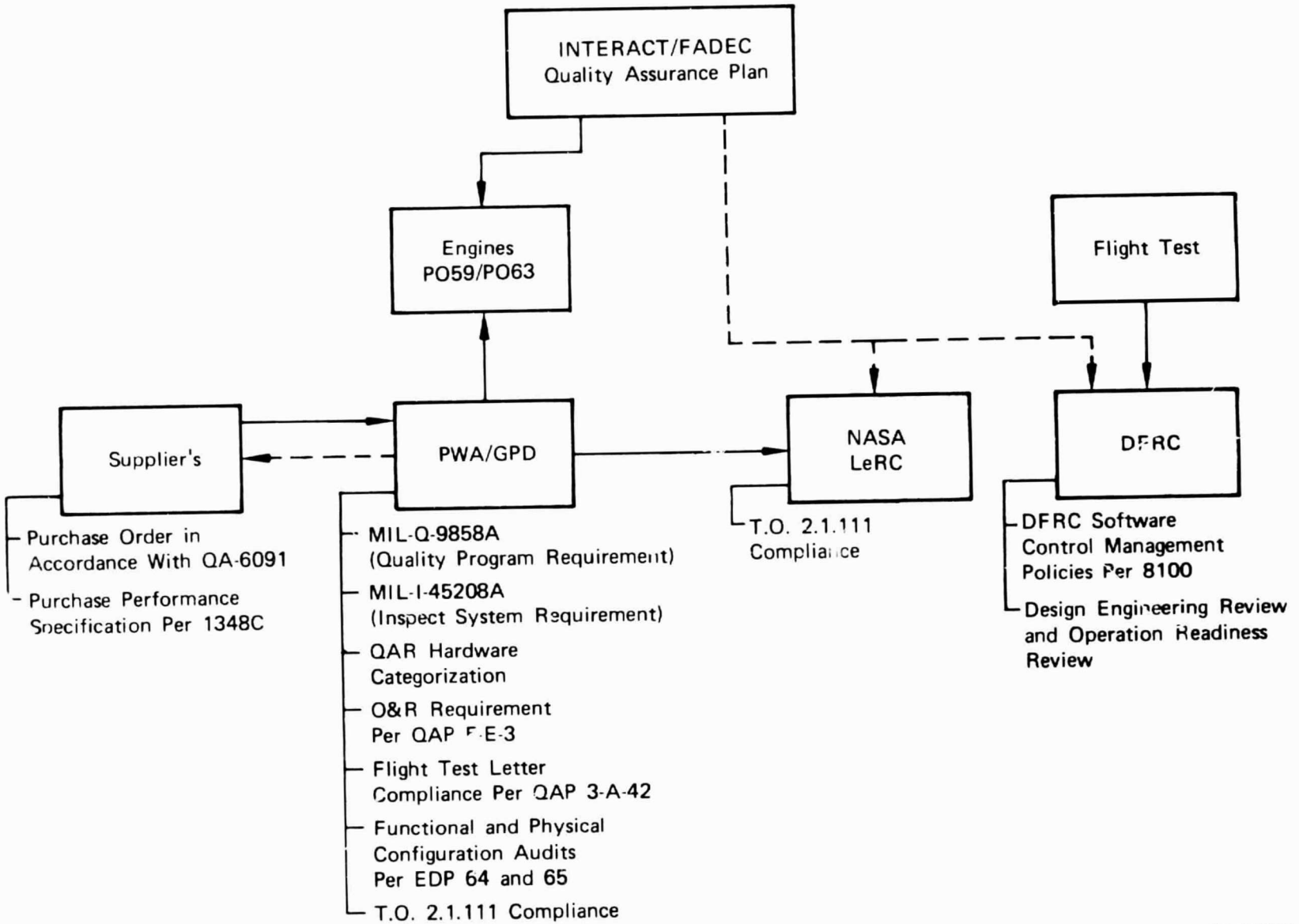

Figure IV-6. INTERACT Quality Assurance Plan Responsibilities

The P&WA F100 engine Quality Program for INTERACT is complemented through Quality procedures which contain the detailed operating instructions. These procedures are subject to review by the resident Government representative. All GFE parts to be used in the INTERACT/FADEC programs shall meet the requirements of MIL-Q-9858A.

NASA DFRC will impose, during the flight test portion of the INTERACT/FADEC Program: (1) software control management policies, (2) design engineering review and (3) Operational Readiness Reviews, as required to insure aircraft safety, and an additional compliance to TO 2.1.111 to maintain flightworthy engines.

3. Records and Reports

P&WA/GPD will utilize Work Instructions as illustrated in Figure IV-7 . Corrective action records of all inspection operations, Material Review Board, and Engineering Reviews on nonconforming supplies will indicate status, trends, deficiencies, and corrective measures taken.

P&WA/GPD shall ensure that records are accessible and retrievable and are maintained as long as required by quality procedures.

4. Engineering Drawings and Changes

The Quality Program provides for control of engineering drawings by a system of checks, approvals, and audits to ensure that a quality design is established. The same engineering drawings used to produce parts for the PFRT and QT engines shall be used to produce prototype parts for INTERACT.

5. Incoming Quality

P&WA has an established system for evaluating and approving procurement sources. Approval of a procurement source is based upon a survey report, the supplier's quality history, or receiving inspection records.

Surveys have been developed for assessment and review of suppliers for adequate assurance of quality. The type of survey performed is based on the complexity, performance, and function of the product, and includes the ability to perform all quality requirements on the parts which the supplier produces. Periodic surveys have been performed to ensure continued compliance with purchase order requirements.

When commercial or off-the-shelf articles and materials or noncomplex, noncritical items are to be procured, a survey of the supplier's facilities is not necessarily required, but Receiving Inspection ensures that the procured articles and materials meet engineering and quality requirements.

When P&WA exercises the prerogative of approving a procurement source based upon quality history or receiving inspection, the local Government representative shall be notified in writing. For all such vendor qualifications under this provision, the Government retains the right of disapproval.

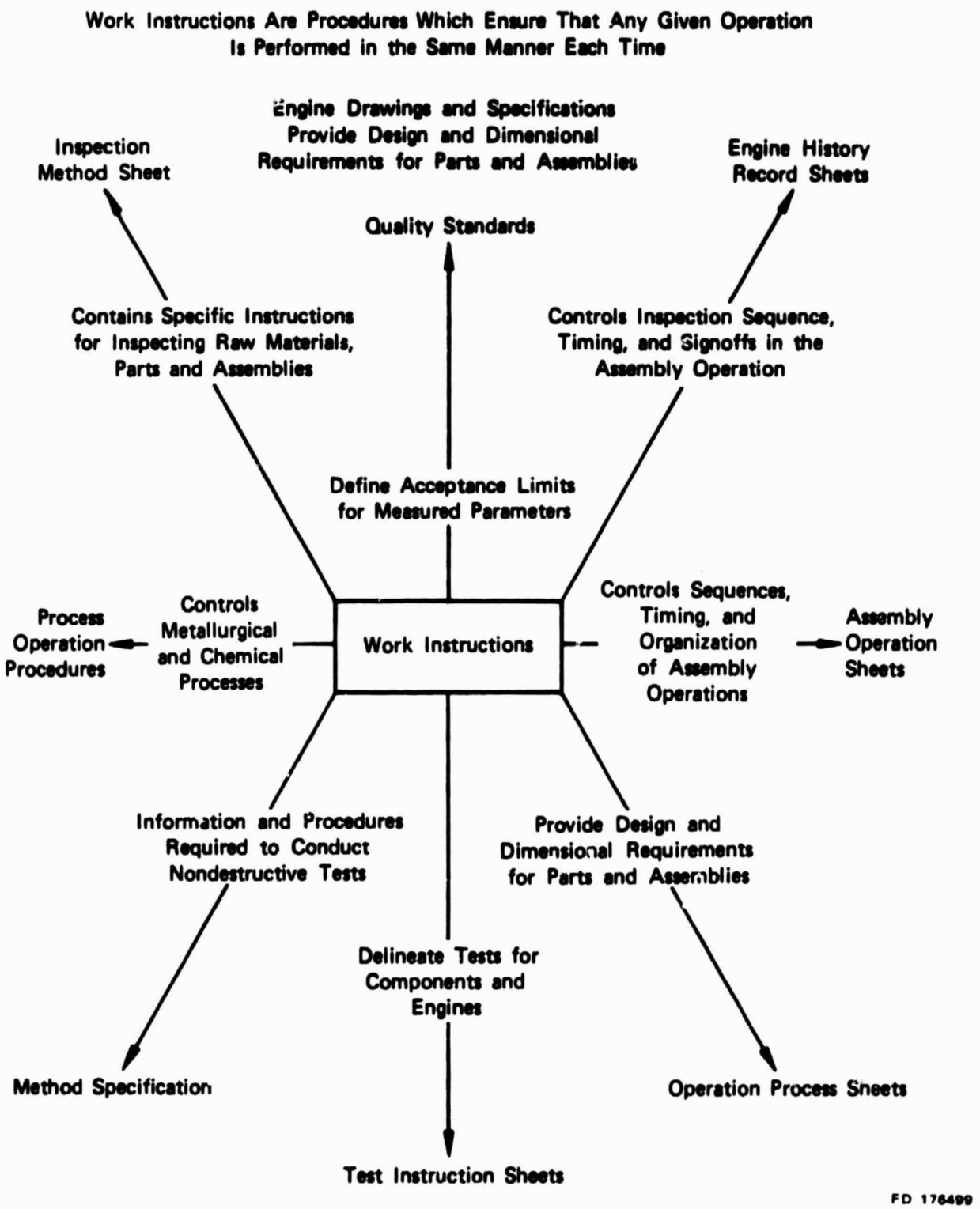

Figure IV-7. Work Instructions

P&WA shall ensure that purchase orders for materials, parts, and assemblies contain all the quality requirements, including Inspection Method Sheets, as required.

P&WA shall perform the required nondestructive tests, dimensional and visual inspections, and Material Control Laboratory testing upon receipt at P&WA.

P&WA shall determine the inspection requirements for development parts. The requirements vary from limited inspection of critical dimensions to full inspection, depending upon the intended use. The requirements and nonconformances, if any, are documented and such parts are identified with appropriate symbols to restrict their use to the intended development testing.

When the complexity of the part or assembly warrants, P&WA assigns a resident Quality representative at the vendor's plant to ensure that all purchase order and quality requirements have been met.

P&WA maintains a vendor rating system whereby each vendor is graded on the quality of the parts produced. When the rating falls below an acceptable level, corrective actions to improve the performance level must be attained or the vendor is removed from the approved source list. Vendor rating reports are issued monthly and furnished to the Purchasing Department. Copies of these reports are given the Government Quality Representative for his information.

Figure IV-8 indicates the flow of material from the supplier through Receiving Inspection to Stores.

6. Manufacturing Control

Quality Engineering shall analyze the manufacturing requirements to identify those points at which inspection controls must be established for each engine item and document the necessary control procedures on work instructions.

The Quality Program shall utilize process inspection when examination of the finished item alone does not provide an adequate evaluation of the quality of the manufacturing processes involved. Control over these processes shall be established to ensure conformance to the applicable P&WA specifications, Aerospace Material Specifications, and Process Operation Procedures. Quality Assurance shall verify that in-process manufacturing operations have been satisfactorily completed before any further processing is performed. Upon completion of fabrication, each item will be inspected to ensure compliance with all engineering drawing and Inspection Method Sheet requirements. Production items shall be identified with the P&WA final acceptance symbol. Development items will be identified with an appropriate development inspection symbol which will limit their use for development testing only. Nonconforming items will be segregated and submitted to the Materials Review Board for investigation and disposition.

On development parts, the Development engineer may require manufacturing operators to dimensionally inspect the operations they perform. These inspections shall be documented on the work orders. Prior to final acceptance, the Inspection department shall verify that all inspection operations have been completed and all nonconformances are documented on quality review forms. The parts shall be identified with appropriate symbols to limit their use for development testing.

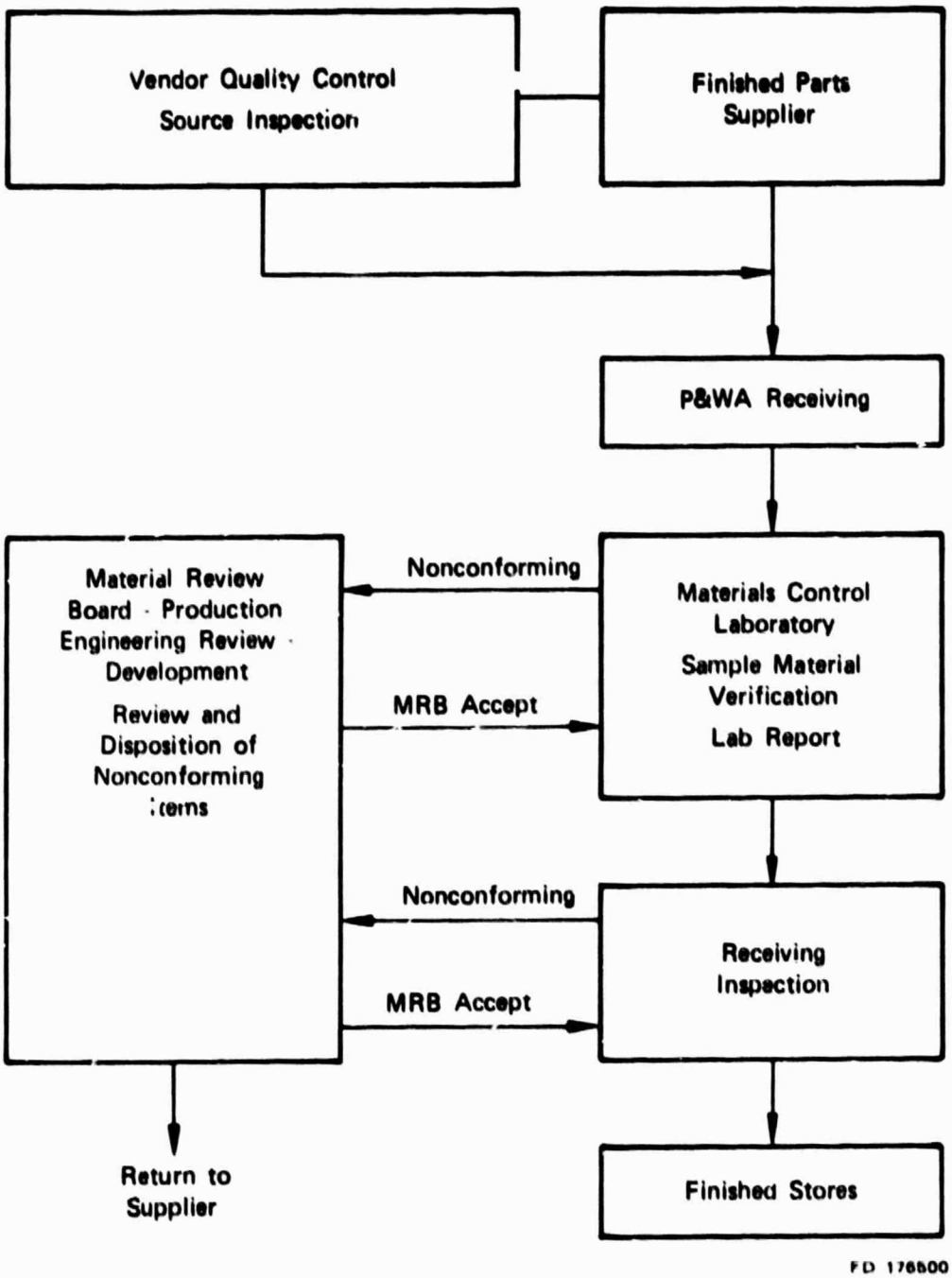

Figure IV-8. Quality Control from Supplier to Stores

Assembly Quality Assurance shall utilize Assembly Operation Sheets, Assembly Procedures, Engineering Instructions, and Engine History Record Sheets to ensure that each engine is properly assembled in accordance with the engineering drawings, flight test letters, or to the Bill-of-Material configuration.

Test Quality Assurance shall witness each INTERACT/FADEC engine and component test to verify compliance with engineering design requirements and to ensure that the performance characteristics of the approved engine configuration have been met. In addition, test inspectors shall witness engine and component repairs and adjustments performed in the Test area to ensure conformance to applicable assembly specifications and procedures.

Completed engine and component assemblies shall be preserved prior to shipment in accordance with instructions contained in Engineering Instructions and Test Instruction Sheets. Quality Assurance shall witness these operations and document compliance in the Engine Inspection Record. Packing Instructions for engine and component assemblies shall be delineated on Assembly Operation Sheets, and compliance with these instructions shall be verified by Assembly Quality Assurance and documented on Engine History Record Sheets. Quality Assurance shall assure that packing and shipping of engines and component assemblies are performed in accordance with the requirements of the contract.

7. Nonconforming Material

P&WA/GPD shall maintain positive control of nonconforming material through identification, segregation, and retention in controlled areas.

All nonconformances shall be documented on applicable material review forms. Nonconforming material shall be segregated prior to disposition to prevent its unauthorized use. Each nonconformance shall be investigated to determine the cause, responsibility, effect on engine use, and corrective action initiated.

Production engine part nonconformances shall be submitted to the Material Review Board for final disposition. The Government representative will have final authority for approval/disapproval of all Material Review Board actions. P&WA shall mark accepted engine nonconforming materials with special identifying symbols. This material will be authorized for use in any production engine, assembly, or spare part. Scrap material shall be permanently marked with a reject symbol or mutilated.

Development engine part nonconformances shall be documented on applicable Quality Review Orders and submitted for investigation to the Material Review Board responsible for development parts. The Quality Assurance and Government Representative members of the MRB shall be advised of the nonconformance and participate in the investigation, but disposition of nonconforming development material shall be the sole responsibility of the authorized development engineer member of the MRB who will document his reason for acceptance on the Quality Review Order. The engineer may accept, repair, or reject the part based on his knowledge of the part use. P&WA shall mark accepted development engine nonconforming material with special identifying symbols which will limit the use of parts so marked to development testing only. Scrap material shall be permanently marked with a reject symbol or mutilated. Copies of Development quality review tickets shall be furnished to the Government Representative for information purposes.

8. Inspection Status and Marking

The P&WA quality program shall maintain a system for identifying the inspection status of production engine items and material from the time of receipt through fabrication and assembly.

Unique symbols identifying the inspector of production engine items and material shall indicate completion of nondestructive tests, completion of manufacturing processes of nonconforming material or items by the Material Review Board, and final acceptance. The final acceptance monogram is a registered trademark and shall appear on all INTERACT engine parts, where practical, to indicate that all quality requirements have been met.

Development engine items and material shall be identified with appropriate development symbols identifying the inspector to indicate nondestructive tests, acceptance of nonconforming material by the development engineer, and final acceptance. Traceability will be provided, when size of part permits, by marking each development part with the month and year the part was accepted and with the work order number for shop manufactured parts or purchase order number for purchased parts.

9. Special Quality Assurance Procedures

Inspection of Development Parts for Use in INTERACT F100 Flight Test Engines – This procedure, QAP 3-A-42, does not apply to production parts with a P&WA monogram. A Flight Test Letter (FTL) will be prepared to authorize the installation of development parts on flight test engines to define the flight test requirements and to provide disposition of the parts after test. The FTL shall be approved by F100 Flight Test Engineering and the F100 Operations and Support Manager, with a copy to Quality Assurance and the resident Government representative.

Overhaul and Repair (QAP 5-E-3) – Overhaul and repair requirements for F100/INTERACT engines, modules components, and items are established in Delivery Order Supplements (DOS) issued by Product Support O&R Engineering. DOS authorizes the inspection and repair work required and will also specify the applicable Technical Order Manual (TO) necessary to perform the requested operations, and will indicate the Engineering Changes, Service Bulletins, Service Test Letters and Flight Test Letters to be incorporated.

SECTION V
ENGINE CONTROL COMPONENT REQUIREMENTS

SECTION V
ENGINE CONTROL COMPONENT REQUIREMENTS

The baseline control systems configured for the INTERACT with FADEC Flight Test Program are shown in figures V-1 and V-2. The arrangement is comprised of Electro-Hydromechanical Interfaces (EHMI) and special electrical components, sensors, and probes. Bill of Material (BOM) F100 components are retained where no special configurations are required. All the control system computations will be executed by either the engine-mounted electronic control (FADEC) or by an airframe-mounted programable computer (RPC). A hydromechanical gas generator backup control is also incorporated for added flight safety. The backup control can be automatically switched on by the engine controls, or manually selected by pilot action.

The basic engine control sensing points and outputs are shown in figure V-3. Engine-mounted sensors provide pressure, temperature, and speed signals to the engine controls which convert the information into scheduled outputs, such as fuel flows and variable geometry to provide stable engine operation throughout the flight envelope. Table V-1 shows a list of the engine-mounted control components for the proposed baseline control system configuration.

The location of the various components for INTERACT will not be finalized until aircraft installation requirements have been completed.

Table V-1. Control System Components

EHMI	*BOM*
GG Control	MFP
Aug Control	AFP
CENC	A/I Valve
Aug Pump Controller	P&D Valve
RCVV Actuators (2)	S/B Cylinder
CIVV Master Actuator	N1 Sensor
CIVV Slave Actuator with F/B	T_{T2} Sensors (2)
RCVV F/B Cable	FTIT Sensors (7)
H/M T_{T2} Sensor	Nozzle Actuation System
	Ignition System
	BOM Electrical Cables
Special Electrical Comp's	
Generator	
Special Electrical Cables	*Special Sensors and Probes*
FADEC and RPC Computers	P_{S2} Noseboom Probe
Converter Box	EPR, PB Sensor Box (Req'd for RPC)
Optical Components	
Fiber Optic Data Links	

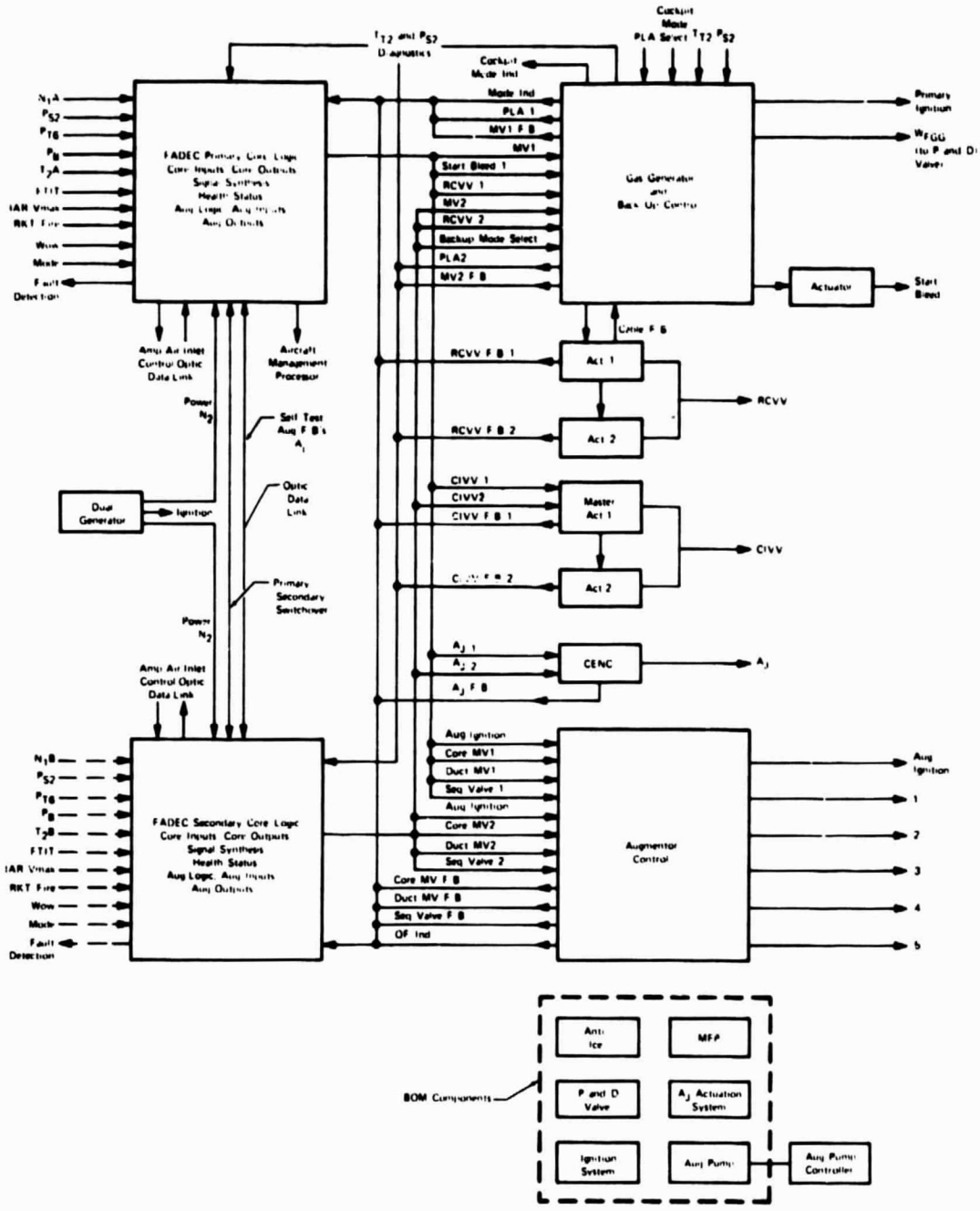

Figure V-1. INTERACT with FADEC Dual FADEC Control System Schematic

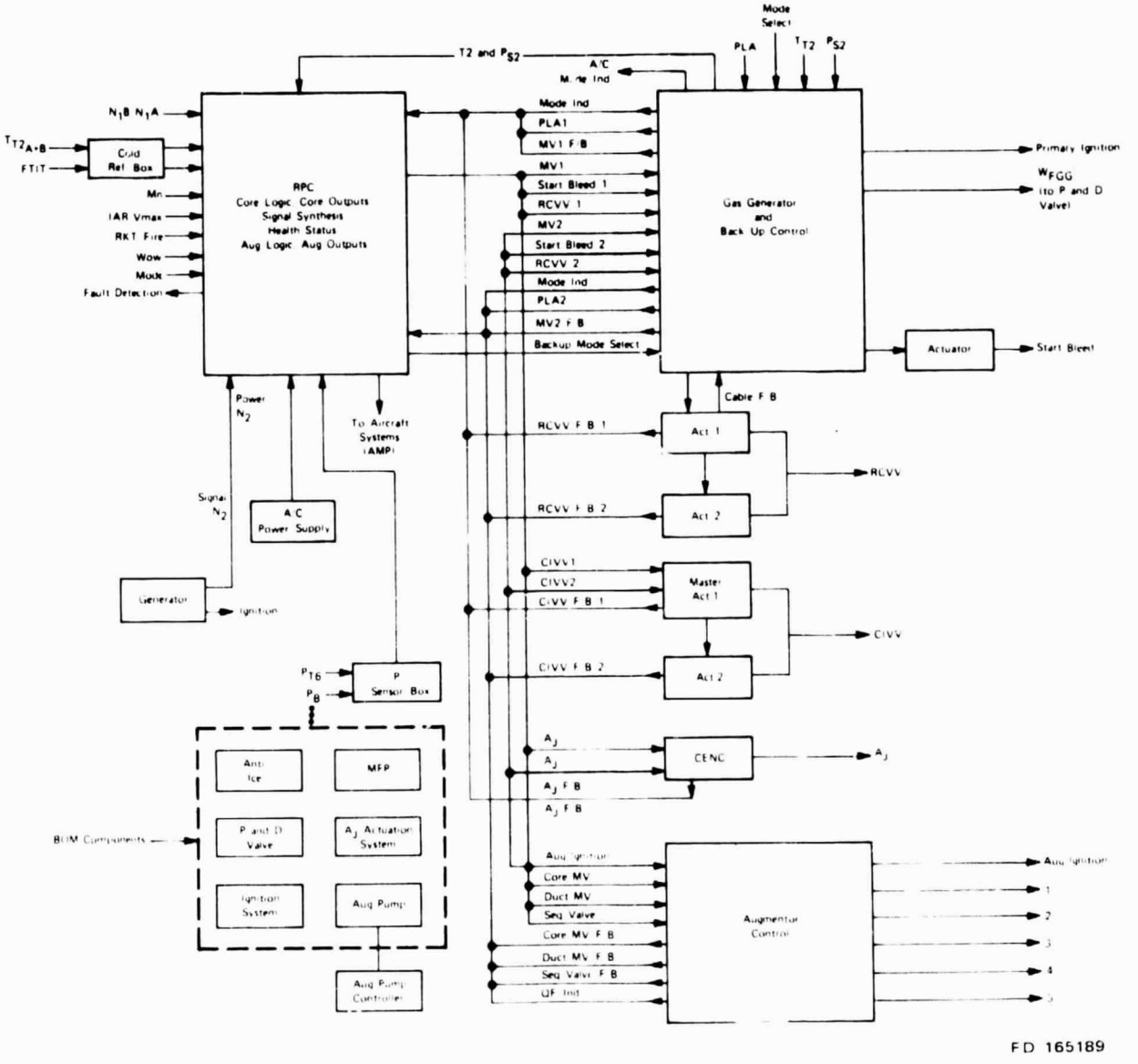

Figure V-2. INTERACT with RPC Baseline Control System Schematic

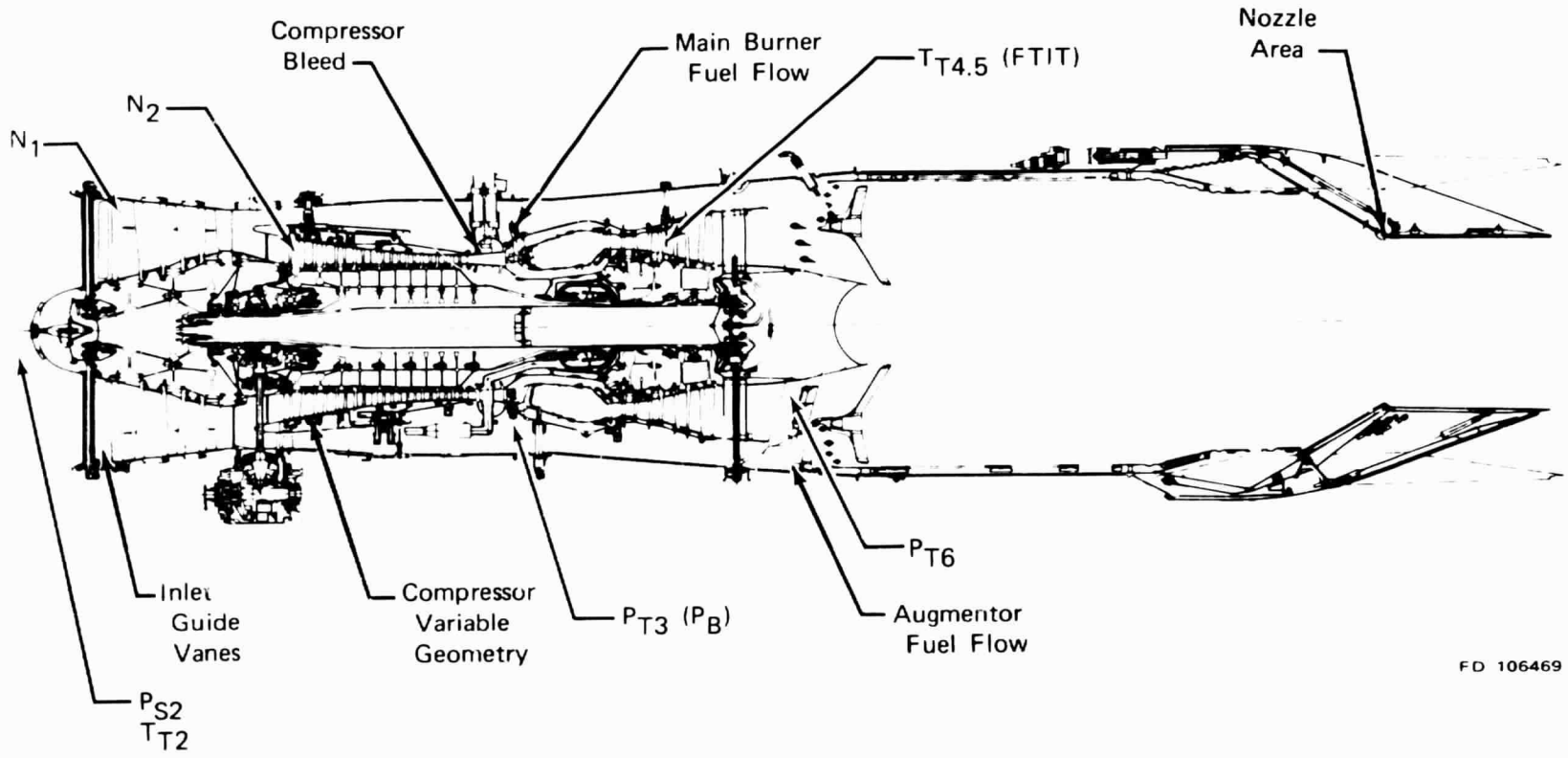

Figure V-3. F100 Control Outputs and Sensing Points

A. ELECTRO-HYDROMECHANICAL INTERFACES (EHMI)

1. Requirements

The EHMI shall provide for actuation of all engine variables by either the FADEC or the RPC through dual torque motor coils. Independent resolver measurements are required of all actuators except for those in the augmentor control. Actuation range and dynamics shall be sufficient to control engine operation from startup through full augmentation over the F-15 flight envelope.

The EHMI shall provide a cockpit-selectable backup control mode whereby the gas generator shall be on hydromechanical control with the other actuators in a safe position. This mode shall be selectable at any flight condition, shall minimize the possibility of engine damage, and provide aircraft fly-home capability.

Cockpit advisories and mode select capabilities shall be coordinated with the integration contractor.

2. General Description

The EHMI components interface with the FADEC or the RPC computers and transform electrical commands from these computers into actual engine control actions. To accomplish this, the hydromechanical components incorporate solenoid valves to translate discrete electrical commands into discrete mechanical positions and electrohydraulic servo valves (EHV) to translate proportional electrical commands into proportional mechanical motion. The EHV's are a two-stage valve design with an electrically-controlled hydraulic amplifier first stage driving a three or four-way spool valve hydraulic second stage. To provide feedback of component position to the computers, position resolvers are used.

3. Gas Generator Control

The gas generator control consists of a combination electro-hydromechanical unit designed to operate in conjunction with the FADEC or RPC computers under normal operating conditions, and provide a hydromechanical back-up system in event of malfunction of the electronic control system. Figure V-4 shows the control input/output diagram.

In the primary mode of operation, the gas generator control provides the following functions:

1. Metered fuel flow to the gas generator, as scheduled by FADEC or RPC
2. RCVV positioning, as scheduled by the FADEC or RPC
3. Engine compressor bleed opening and closing, as scheduled by the FADEC or RPC

4. Supplies the mechanical power lever input position (PLA) to the FADEC or RPC by means of two resolvers

5. Gas generator ignition turn-on/turn-off by means of an electrical switch actuated by the mechanical power lever input

6. Fuel cutoff or turn-on to the gas generator hydromechanically as a function of the mechanical power lever input

7. Supplies filtered fuel for "Muscle" to the Compressor Inlet Variable Vane Control (CIVV) rear compressor variable vanes (RCVV), the Convergent Engine Exhaust Nozzle Control (CENC), and the Augmentor Pump Controller

8. Provides an electrical signal to indicate malfunction and/or failure of either of the backup servo systems and identifies which system is malfunctioning.

In the backup mode of operation, the gas generator control provides the following functions:

1. Meters fuel to the gas generator

2. RCVV positioning

3. Automatic engine starting

4. Fuel cutoff or turn-on to the gas generator

5. Gas generator ignition

6. Supplies filtered fuel flow to other control components

7. Supplies a fuel pressure signal to the augmentor control and the CENC to shutdown the augmentor and close the engine exhaust nozzle

8. Supplies an electrical signal to indicate backup mode operation.

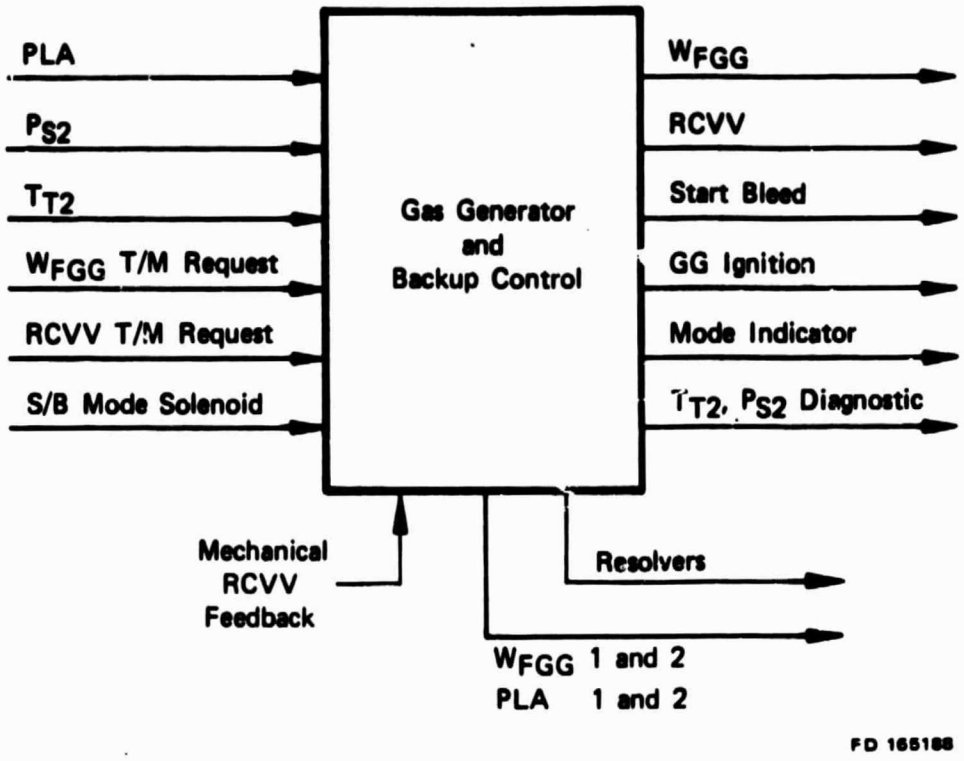

Figure V-4. Gas Generator Control I/O

4. Augmentor Control

The augmentor control combines the augmentor fuel flow metering system, manifold quickfill system, and the distribution system into a single modular-constructed control operated by the FADEC or RPC. Figure V-5 shows the control input/output diagram.

The following characteristics and functions are provided by the Augmentor Control:

1. The distribution system utilizes five 3-position segment valves currently used in the F100 Unified Fuel Control

2. The segment valves, three supplying fuel to the core zone and two supplying the duct zone, are individually positioned in the cutoff, manifold prefill, or metered flow position per command of the segment selector valve

3. A four-way EHV positions the segment selector valve upon request of the FADEC or RPC

4. Position of the selector valve is fed back to the FADEC or RPC by a resolver

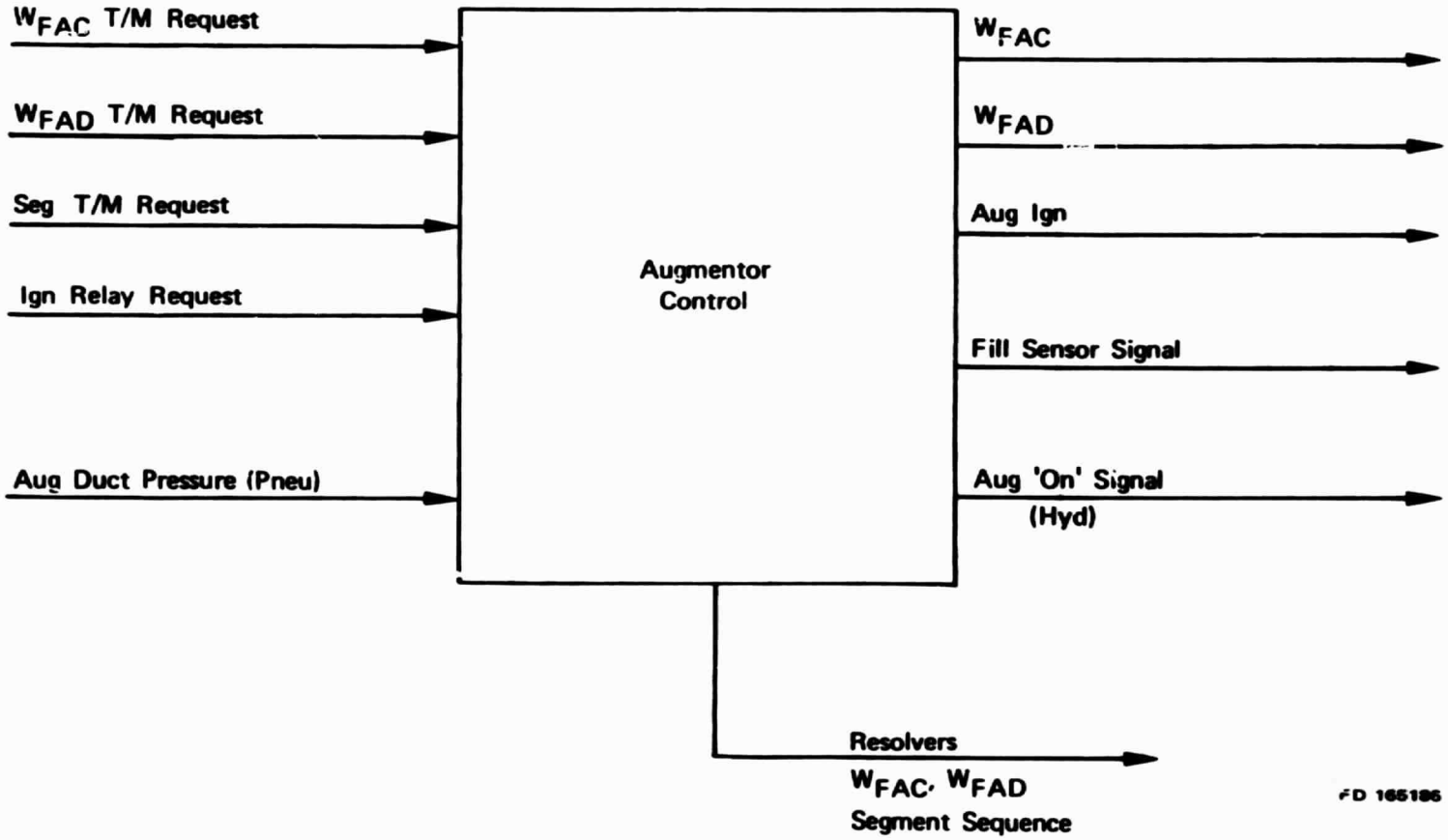

Figure V-5. Augmentor Control I/O

5. The metering system consists of two separate, but identical, core (Segments I, II, and IV) and duct (Segments III and V) metering valves (M/V)

6. The FADEC or RPC independently schedule the two metering valves to supply proper augmentor fuel flow by inputing commands to each of two EHV's

7. The quickfill system, consisting of a fill valve, a fill detector, and an electrical fill detector position switch is similar to that used in the F100 Unified Fuel Control.

5. Convergent Exhaust Nozzle Control (CENC)

The Convergent Exhaust Nozzle Control (CENC) shown in figure V-6 positions the jet nozzle in response to commands from the FADEC or RPC and exhibits the following functions and characteristics:

1. The CENC consists of a reversible air motor, a bidirectional control valve, a mixing transmission, a power piston, a four-way EHV, a resolver, a counter, and an Exhaust Nozzle Position Transmitter (ENPT)

2. The power-producing element of the CENC consists of reversible, high-pressure helical gear motor and bidirectional pneumatic control valve which ports compressor discharge air to one side of the motor while venting the other side to atmosphere

3. A mixing transmission provides direct mechanical feedback between the pneumatic motor position and the air control valve as a function of input nozzle area (A_j) request

4. An electrohydraulic four-way servo valve (EHV) driving a power piston provides the A_j request input to the mixing transmission

5. The EHV is biased to provide a fail-safe failure mode in the closed nozzle direction upon loss of current

6. Power piston position (A_j request) and feedback (electrical) is supplied to the FADEC and RPC by a resolver

7. To facilitate rigging the nozzle and CENC, the CENC has a digital counter which is driven by the air motor geartrain

8. The ENPT is also driven by the motor geartrain and provides the pilot with an indication of nozzle position

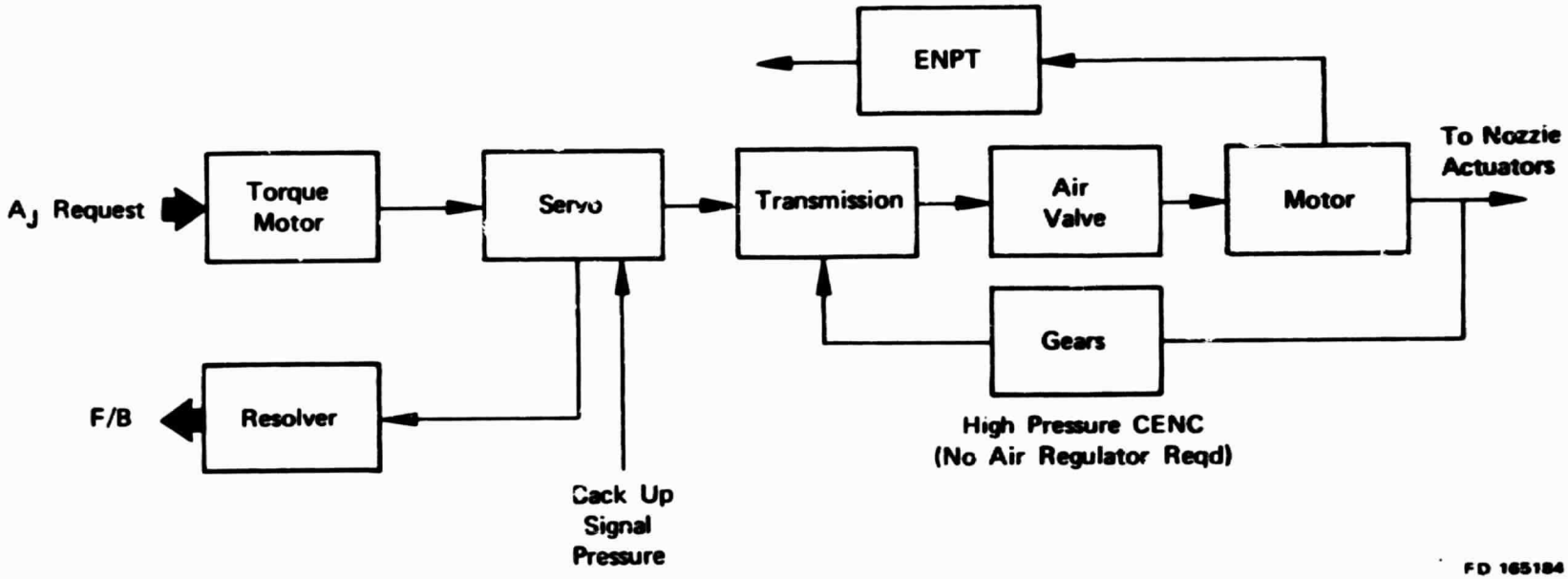

Figure V-6. CENC Functional Block Diagram

9. An orifice-check valve arrangement is provided to limit power piston velocity in either direction of travel and thus prevent overshoot, damage, and/or instability in cases of large A_j request

10. Upon transfer to backup mode, the gas generator control provides a signal to a logic valve which moves the power piston and, therefore, the exhaust nozzle to the minimum open position

11. The CENC : nnected to the exhaust nozzle through a transmission system cons of two flex drive shafts, flexible drive loop, and five ballscrew ac. .s (see figure V-7).

6. Augmentor Pump Controller

The augmentor pump controller (figure V-8) mounts on the augmentor fuel pump and modulates the airflow to the pump turbine, thereby controlling its speed. Controller design and operation includes:

1. Controls the speed of the augmentor pump to provide the design metering valve head to the augmentor control while satisfying the flow requirement

2. The reference pressure used for control is the higher of the two augmentor metered flow discharge pressures (P_{F3AD}, P_{F3AC})

3. The difference in the reference pressure and augmentor inlet pressure (P_{F1AW}) is the controlling pressure

4. This controlling pressure drives a nutcracker linkage and servo which positions a double-diameter piston, which in turn drives the pump turbine air valve

5. Servo pressure (P_{FS}) and body pressure (P_{FCB}) are the operating pressures for the piston

6. The gain of the nutcracker servo is varied as a function of burner pressure (P_B)

7. An overpressure limiter is incorporated to limit augmentor pump discharge pressure in the event of a malfunction.

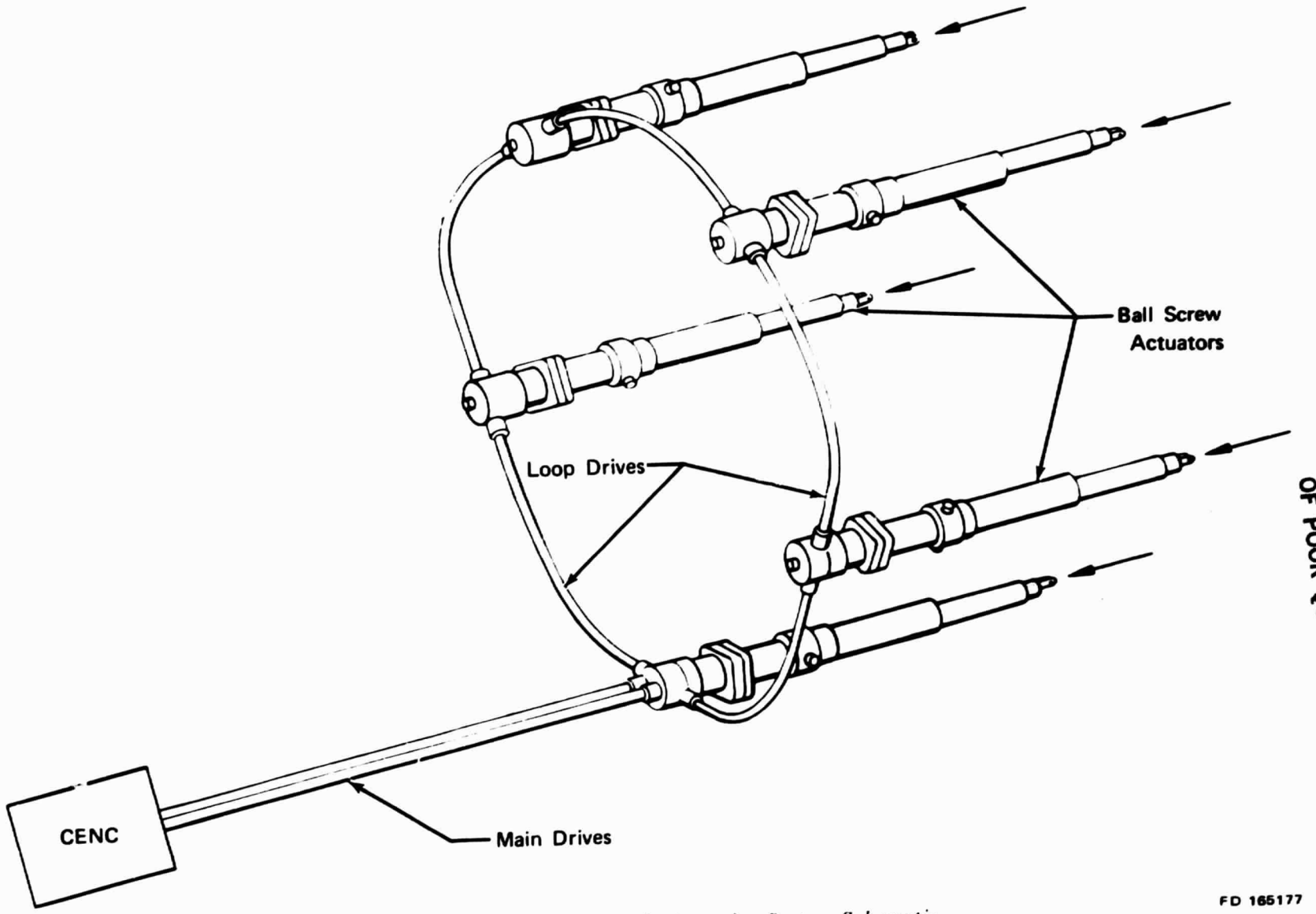

Figure V-7. Exhaust Nozzle Actuation System Schematic

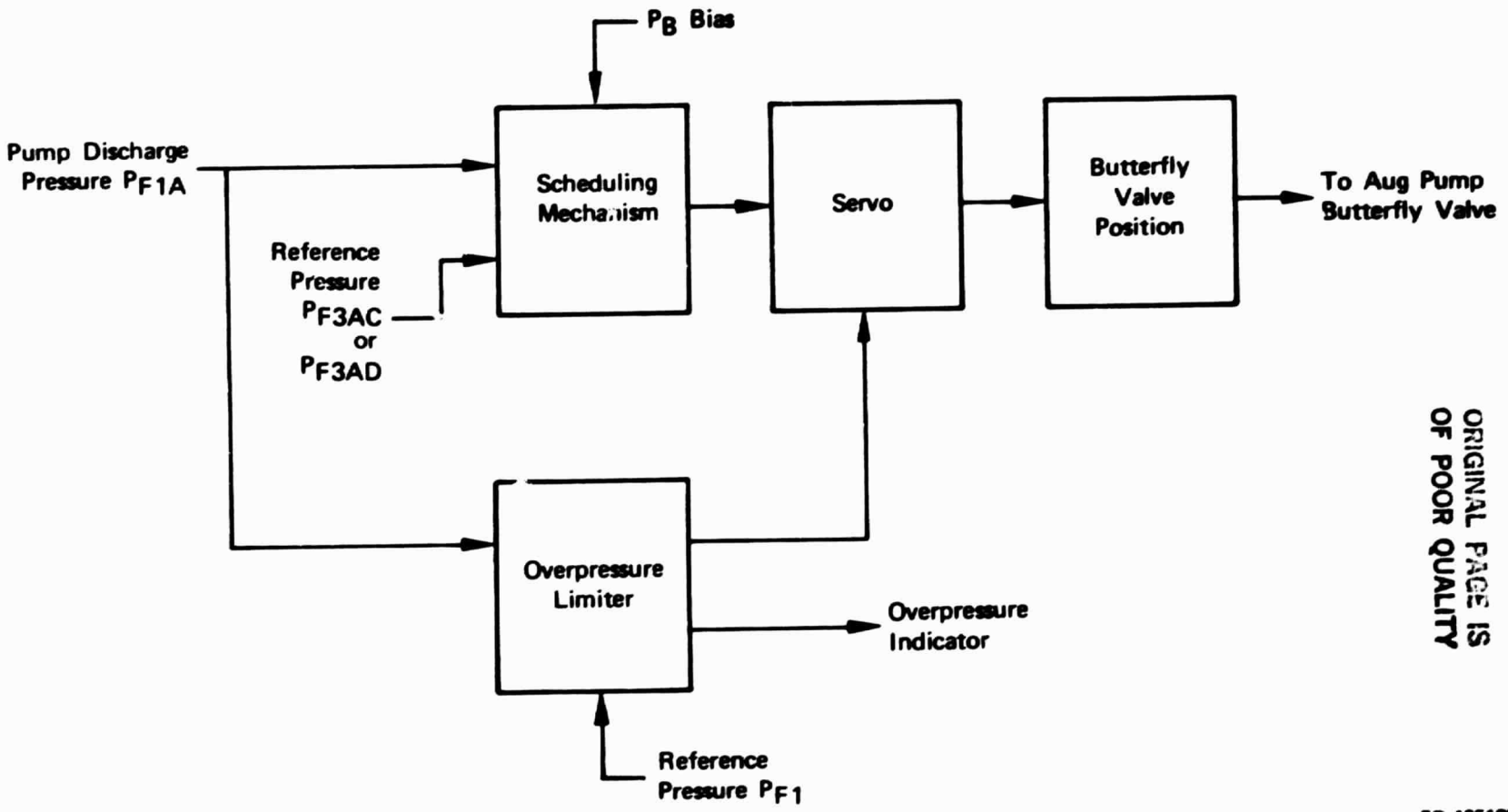

Figure V-8. Augmentor Pump Controller Functional Block Diagram

7. Rear Compressor Variable Vane (RCVV) Actuators (Two Per Engine)

The RCVV actuator shown in figure V-9 is a hydraulic cylinder used to rotate the inlet stator vanes on the turbofan engine rear compressor. Each engine installation requires two RCVV actuators, both of which are identical. The actuator power piston is driven by fuel pressure supplied by a four-way electromechanical servo valve located on the gas generator control. This servo valve is controlled by an electrical signal from the FADEC or RPC during primary control operation. A resolver linked to the power piston shaft on each actuator provides positioning feedback to the computers, closing the control loop. When operating the engine in the hydromechanical back up mode, a mechanical indication of RCVV position is fed back to the backup control.

8. Compressor Inlet Variable Vane (CIVV) Control

The CIVV control system shown in figure V-10 consists of two hydraulic cylinders. One cylinder is the master actuator containing the control components while the second is a slave actuator. A four-way electrohydraulic servo valve (EHV) mounted on the master actuator provides the fuel pressure to position both the master and slave power pistons. The servo valve is controlled by a signal from the FADEC or RPC.

The CIVV slave actuator is a hydraulic cylinder controlled by the servo valve which is part of the CIVV control master actuator assembly. The same pressures supplied to the master actuator power piston are supplied to the slave power piston causing the two to work in unison.

Each actuator contains a resolver linked to the piston shaft to provide feedback to the FADEC and RPC.

The CIVV's are set to the cambered p ation during backup control operation.

9. Hydromechanical T_{T2} Sensor

The hydromechanical T_{T2} sensor probe mounts on the engine inlet and provides a pressure signal to the temperature receiver in the gas generator control. This pressure signal is proportional to engine inlet total temperature T_{T2}. The temperature receiver mounts directly in the gas generator control and provides a T_{T2} input to the backup controls schedules.

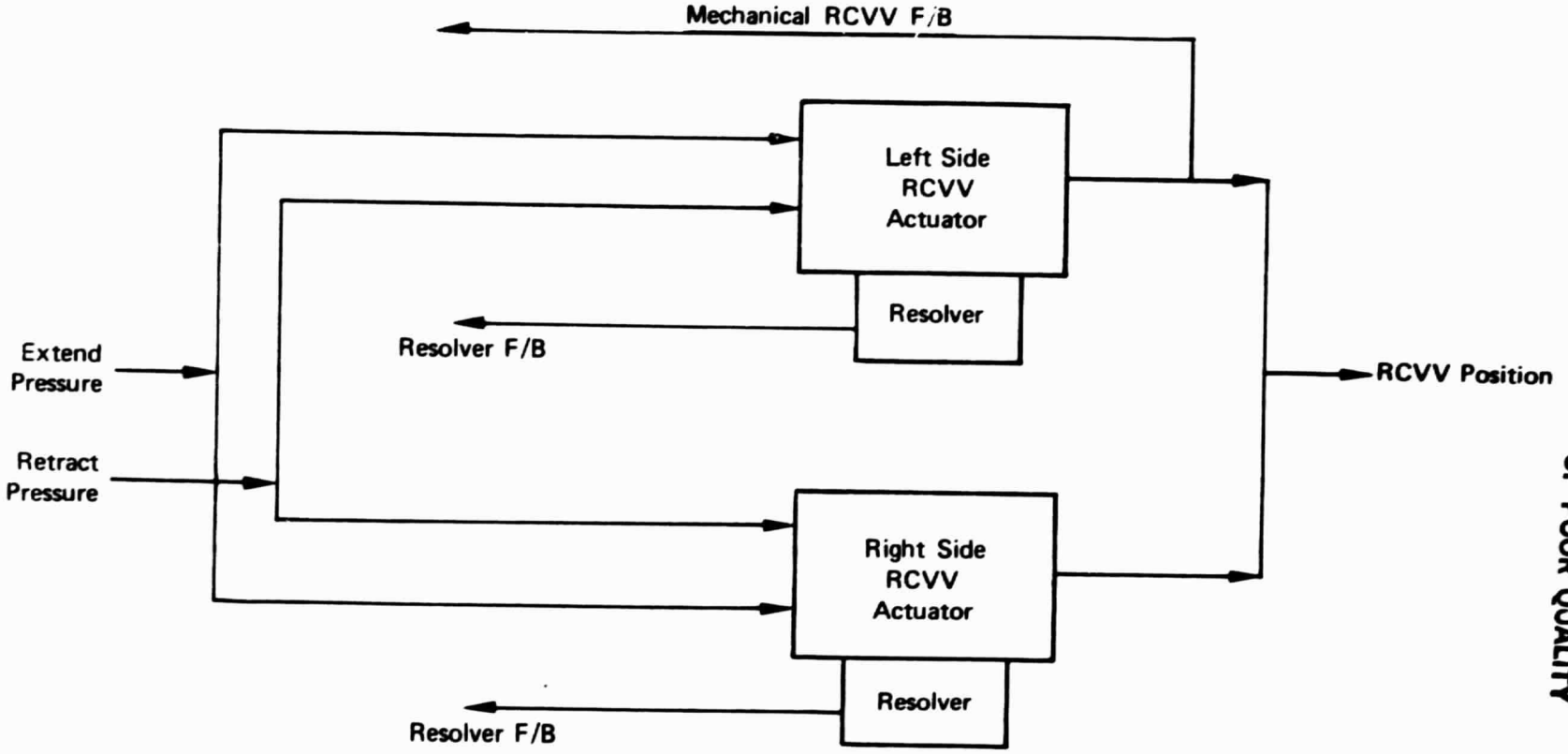

Figure V-9. RCVV Actuation System Functional Block Diagram

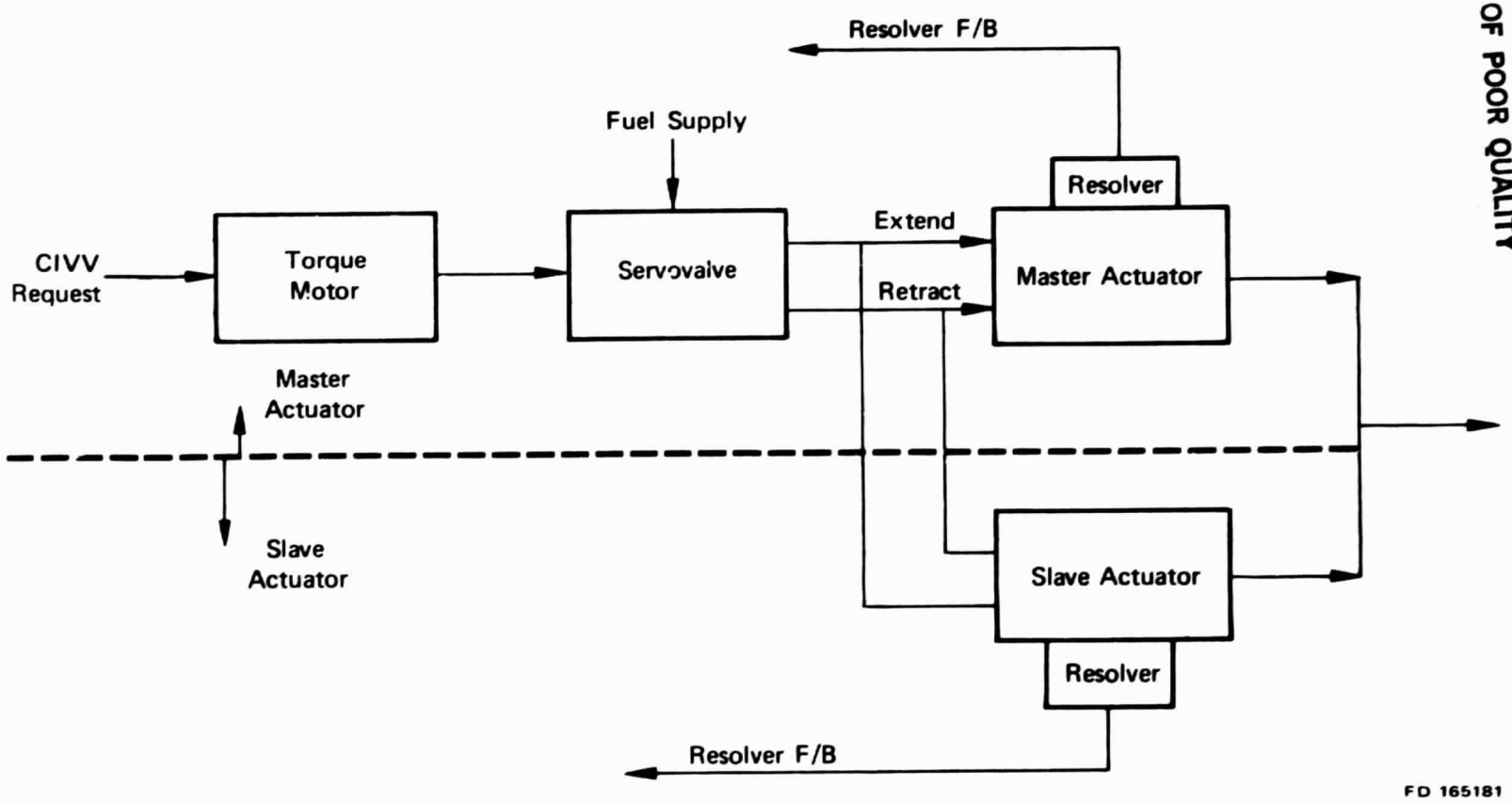

Figure V-10. CIVV System Functional Block Diagram

B. BILL-OF-MATERIAL COMPONENTS

1. Main Fuel Pump

The main fuel pump consists of an integral dual-element configuration with a centrifugal boost stage and a fixed-displacement vane stage.* The boost stage supplies pressurized fuel to the main fuel pump vane stage and to the augmentor fuel pump, when an augmentation permission signal clutches in a high flow centrifugal flow element. High-pressure fuel from the vane stage is delivered to the gas generator control and provides hydraulic servo muscle for the variable-geometry actuators. The gas generator bypass valve, located on the gas generator control, regulates flow output to maintain a constant pressure drop across the gas generator metering valve. The boost pump and gas generator vane pump are mounted on the same shaft and directly driven by the engine gearbox.

A functional block diagram of the main fuel pump is shown in figure V-11.

2. Augmentor Fuel Pump

The augmentor fuel pump provides fuel flow to the augmentor control for quickfill and metered flow distribution. This pump is a single-stage centrifugal pump driven by an air impulse turbine. A butterfly valve, located in the air inlet line, controls pump speed by regulating turbine air supply. During non-augmentation engine operation, the butterfly valve is closed to minimize fuel temperature rise and improve specific fuel consumption.

A functional block diagram of the augmentor fuel pump is shown in figure V-12.

3. Anti-Icing Valve

The engine inlet anti-icing valve directs 7th-stage high-pressure compressor bleed air through the inlet guide vane struts into the noseboom probe assembly to prevent ice buildup on the engine inlet. Upon pilot selection, the valve is electrically actuated through a solenoid and pneumatically operated. When the solenoid is de-energized, high-pressure air is directed to the front side of the sleeve valve while the rear side is vented to ambient pressure. The unbalanced pressure plus the spring load opens the valve. Conversely, when the solenoid is energized, the front side of the sleeve is vented to ambient pressure and the unbalanced pressure closes the sleeve valve.

4. Pressurizing and Dump Valve

The fuel pressurizing and dump (P&D) valve drains the gas generator fuel manifolds on engine shutdown maintaining a full supply line from the unified control to the pressurizing and dump valve. The valve also ensures adequate backpressure to the gas generator to maintaining proper servo pressure regulation.

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* The BOM F100 main fuel pump utilizes a variable displacement vane stage. For the INTERACT program, the pump will be locked in the "max" flow setting and excess flow delivery will be bypassed by a valve located in the gas generator fuel control.

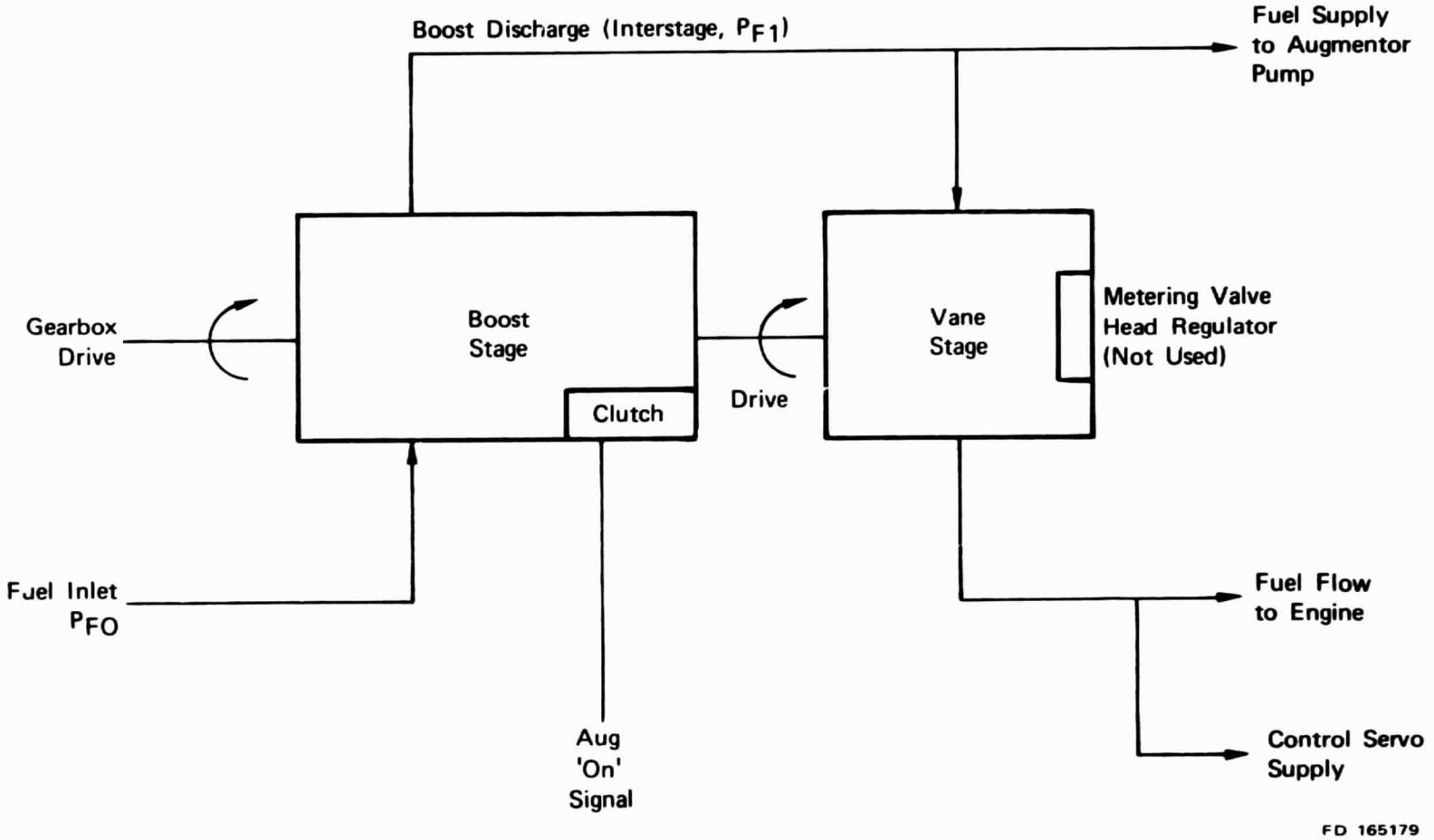


Figure V-11. Main Fuel Pump Functional Block Diagram

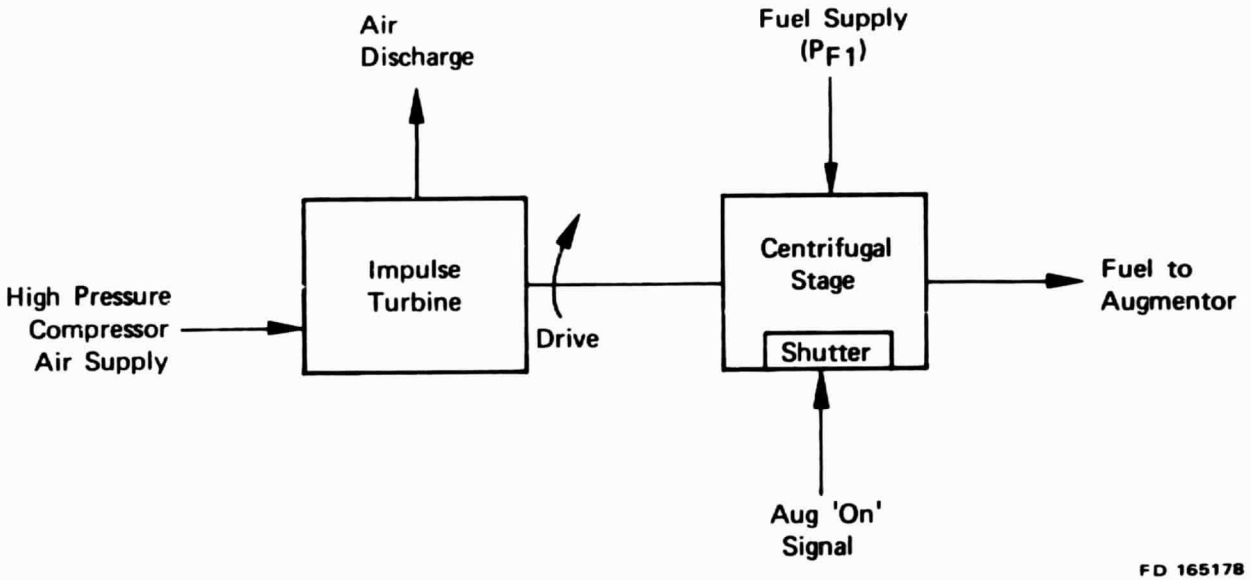


Figure V-12. Augmentor Fuel Pump Functional Block Diagram

5. Start Bleed Cylinder

The start bleed cylinder is engine-mounted for two-position control of the high compressor start bleeds. High and low fuel pressure is alternately provided to both sides of the bleed cylinder by the gas generator control to open or close the bleeds during engine starts.

6. N1 Sensors

The engine assembly contains a dual-coil magnetic sensor which provides redundant speed signals to the electronic control.

Fan rotor speed is also detected by an eddy current sensor that provides an indication of fan speed to ground/aircraft support equipment.

7. T_{T2} Sensors (Two Per Engine)

The engine inlet temperature sensor (probe) shown in figure V-13 consists of two multi-junction chromel-alumel thermocouple sensors units mounted at the engine inlet to provide two inlet temperature signals (millivolt signal) to the engine electronic control.

8. Fan Turbine Inlet Temperature (FTIT) Sensors (Seven Per Engine)

The FTIT measurement system shown in figure V-14 consists of seven dual-junction chromel-alumel thermocouple sensor units, mounted at station $T_{T4.5}$, to provide signals of fan turbine inlet temperature to the electronic control and to the airframe. Two signals representing averages of four and three junctions are provided to the engine electronic control where final averaging is achieved. The $T_{T4.5}$ signal for airframe indication is obtained from the average of the other seven temperature signals at the bulkhead connector panel.

9. Ignition System (Exciters and Igniters)

The ignition exciter is a hermetically-sealed unit which contains either one gas generator ignition circuit and one augmentor ignition circuit (dual exciter) or one gas generator circuit (single exciter). The dual ignition exciter and the single ignition exciter provide a 4-joule stored energy level to each spark igniter for main ignition and a 2.6-joule stored energy level to the spark igniter for augmentor ignition. Electrical power is supplied to each exciter circuit by an electrically-independent winding of the engine self-contained generator.

Spark igniters conduct the high energy potential created by the exciter and allow the energy to discharge across an air gap located at the proper position in the combustion chamber.

The augmentor and gas generator igniters are functionally the same, but differ in physical dimensions to accommodate mounting differences.

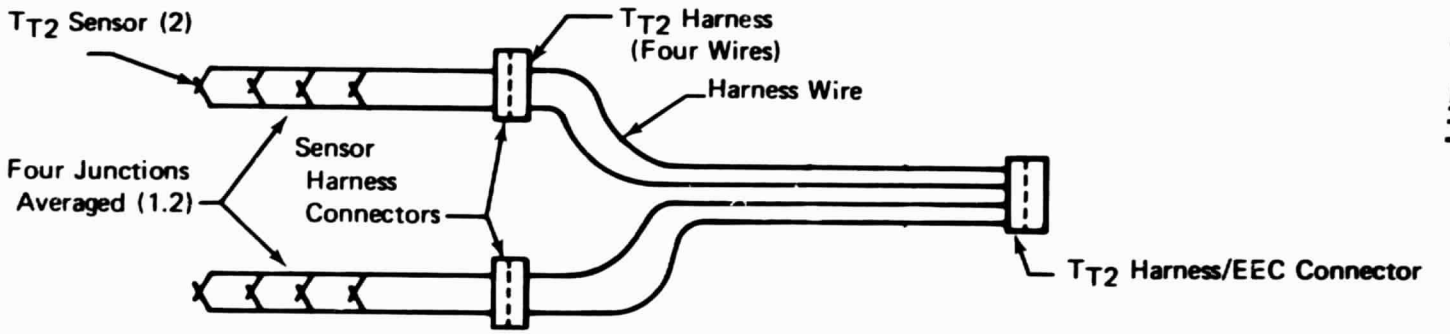


Figure V-13. T_{T2} Sensor Schematic

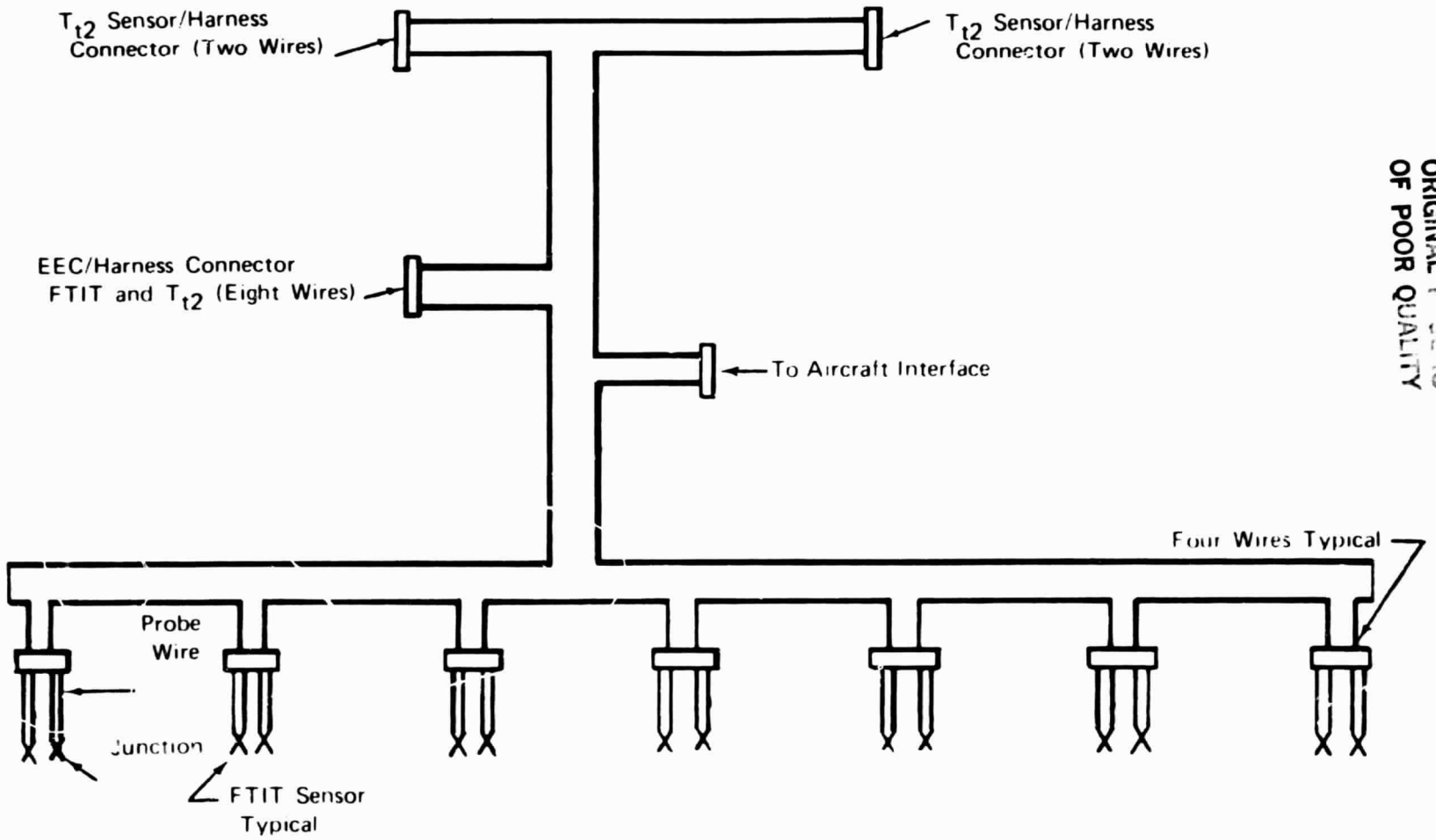


Figure V-14. FTIT Sensor Schematic

10. Electrical Cables

The engine-mounted electrical cables consist of insulated stranded conductors, properly sized and covered by protective metal overbraid and terminated with the proper connectors.

The BOM cables to be retained for this program will be determined after the engine wiring diagram is coordinated with the integration contractor.

C. SPECIAL ELECTRICAL COMPONENTS

1. Generator

The generator stator and rotor mount on the engine gearbox utilizing the gearbox bearings and shaft to provide a permanent-magnet type, engine-driven generator. The generator supplies electrical power for the engine components and provides N2 speed signals to the electronic control and the airframe interface. The generator assembly is comprised of a rotor and a stator. The generator contains the following windings:

1. Two identical nonregulated, single-phase main ignition windings
2. Two identical nonregulated, single-phase augmentor ignition windings
3. One nonregulated, single-phase N2 speed winding to furnish a speed signal to the engine interface
4. Two nonregulated, three-phase windings to furnish power and N2 signals to the electronic controls
5. Two nonregulated, single-phase, low voltage auxiliary windings.

2. Special Electrical Cables and Bulkhead Connector Panel

Electrical cables other than the BOM cables that can be retained will be determined through coordination with the integration contractor.

3. Converter Box

Converter Box requirements to couple FADEC to the aircraft Mil-Std-1553 data bus will also be determined through coordination with the integration contractor.

D. SPECIAL SENSORS AND PROBES

1. P_{S2} Noseboom Probe

The P_{S2} probe provides an engine inlet static pressure signal to the FADEC, RPC and the gas generator controls. The electronic control uses this signal for the primary engine pressure ratio control. The gas generator control uses the signal to bias the fuel flow scheduled to the engine during backup control operation. The probe will replace the BOM F100 engine nose cone.

2. Pressure Sensor Box

Operation of the engine with the RPC control system requires that pressure sensors be incorporated. The number of pressure sensors, locations, and the specific pressure ranges will be coordinated with the integration contractor. Once defined, a box incorporating the required pressure sensors will be identified for use in the INTERACT program.

3. Cold Reference Box

A reference junction for the FTIT and T_{T2} temperature signals will be necessary for the RPC system. The specific location of this box will be coordinated with the Integration Contractor, in addition to specific design criteria for the reference box.

E. OPTICAL COMPONENTS

1. Fiber Optic Data Link

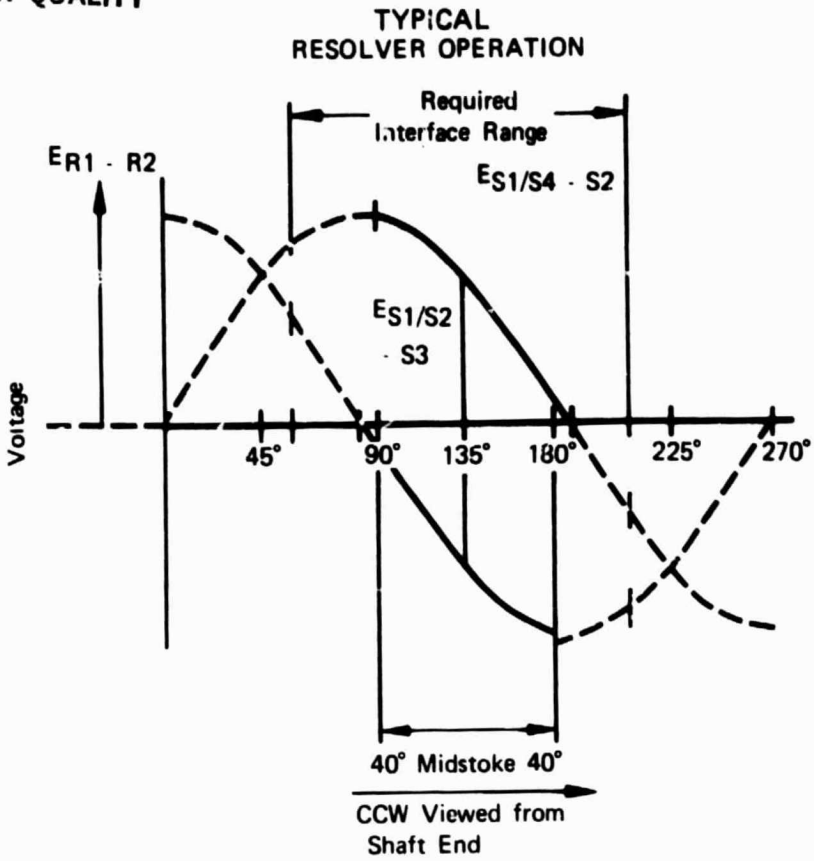
The fiber optic data link is discussed in Section VI.

F. PLUMBING

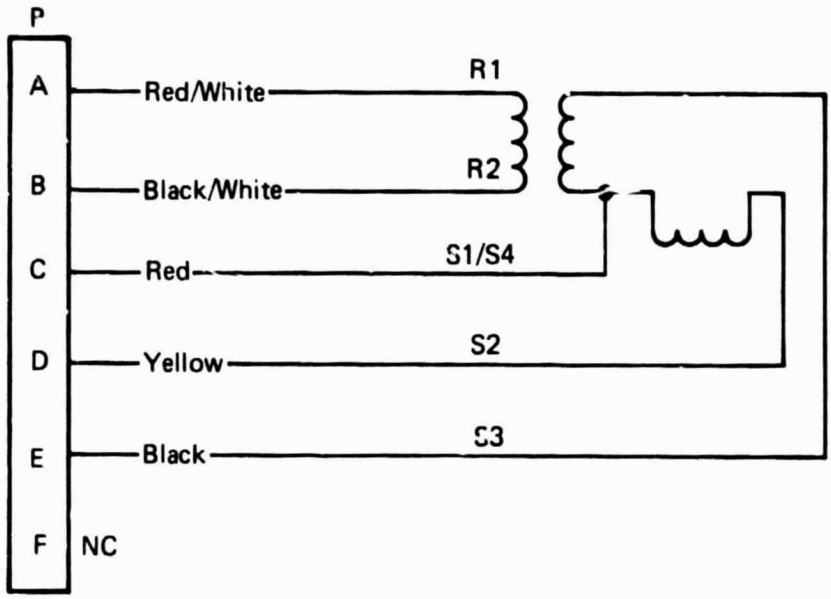
The plumbing required to incorporate the EHMI components in the control system is defined. New requirements for the special added components will be coordinated with the integration contractor.

G. INTERFACE ELECTRICAL CHARACTERISTICS

The electrical characteristics of the EHMI electrohydraulic flow control valves and resolvers are described in figure V-14 and Tables V-2 through V-5.



Resolver Operation



Resolver Wiring Schematic and Code

FD 168058

Figure V-15. Resolver and Servo Valve Electric Characteristics

Table V-2. Electrical Requirements Gas Generater Control

Electrohydraulic Servo Valve Specifications

	Metering Valve	*RCVV*
Rated Current	± 20 ma	± 20 ma
Resistance	160 Ω ± 10%	160 Ω ± 10%
Null Bias	4 ± 0.4 ma	4 ± 0.4 ma
Coil Configuration	Two independent coils	Two independent coils
Max Current	45 ma	45 ma
Inductance	0.5 Henries each coil at 50 hz	0.5 Henries each coil at 50 hz
Hysteresis*	4% rated current (max)	4% rated current (max)
Threshold*	0.5% rated current (max)	0.5% rated current (max)

Solenoid Electrical Characteristics

	Mode	*Compressor Bleed*
Type	2 way	2 way
Voltage	14v	28v
Resistance	63Ω±10 at 77°F	126Ω
Min Dropout Voltage	2v	2v

Mode Indication Switch Characteristics

Voltage	28v
Current	250 ma
Contacts	Double Open = Primary Mode

Diagnostic Switch Electrical Characteristics

Voltage	28
Current	250 ma
Resistance	0.1 ohm

Resolver Electrical Characteristics

Resolver Specifications

	Metering Valve	*PLA*
Primary Voltage	7 volts	7 volts
Primary Frequency	1660 Hz	1660 Hz
Input Current	0.010 amp	0.010 amp
Input Power	0.015 watts	0.015 watts
Impedance ZRO	128 + J650	128 ± J650
Impedance ZSO	18 + J176	28 + J176
Impedance ZSS	23 + J16	23 + J16
Output Voltage	3.5 volts	3.5 volts
DC Resistance (Rotor)	56.8 ohms ± 10%	56.8 ohms ± 10%
DC Resistance (Stator)	7.5 ohms ± 10%	7.5 ohms ± 10%
Phase Shift	5.6 degrees	5.6 degrees
Load	10,000 ohms nominal	10,000 ohms nominal
Range	50° to 200°	97.5 to 172.5°

*As defined by ARP 490C

Table V-3. Augmentor Control Electrical Requirements

Electro-Hydraulic Flow Control Valve Specification

	Metering Valves (2)	*Sequence Valve*
Configuration	2 stage, 3 way	2 stage, 4 way
Coil configuration	Two independent coils	Two independent coils
Rated current	± 20 ma	± 20 ma
Resistance	160 ± 10% ohms/coil	160 ± 10% ohms/coil
Max current	45 ma	45 ma
Inductance	0.5 henries/coil at 50Hz	0.5 henries/coils at 50 Hz
Null bias	−20 ma ± 0.4	−4 ma ± 0.4
Threshold	≤0.25% of rated current	≤0.25% of rated current
Hysteresis	≤4% of rated current	≤4% of rated current

Resolver Specification

	Metering Valves (2)	*Sequence Valve*
Primary voltage	7 volts	7 volts
Frequency	1660 Hz	1660 Hz
Current	0.010 amp	0.010 amp
Power	0.015 watts	0.015 watts
Impedance ZRO	128 plus J650	128 plus J650
Impedance ZSO	28 plus J176	28 plus J176
Impedance ZSS	23 plus J16	23 plus J16
Output voltage	3.5 volts	3.5 volts
DC resistance (rotor)	56.8 ohms ± 10%	56.8 ohms ± 10%
DC resistance (stator)	7.5 ohms ± 10%	7.5 ohms ± 10%
Phase shift	5.6 deg	5.6 deg
Range	75 deg Midstroke at 235°	75 deg Midstroke at 135°

Manifold Micro Switch Specification

Contact	Normally open
Resistance	*
Current	100 ma max
Voltage	28 vdc

* Switch contact resistance shall not exceed 5 ohms with 6 v[illegible] available for film breakdown and contact current limited to 0.5 ma.

Table V-4. CIVV Control and Slave Actuator Electrical Requirements

Electro-Hydraulic Flow Control Valve Specifications (Control Only)

Rated current	±20 ma
Resistance	160 Ω ± 10%
Null bias	4 ± 0.4 ma
Coil configuration	Two independent coils
Max current	45 ma
Inductance	0.5 Henries each coil at 50 Hz
Hysteresis*	4% rated current (max)
Threshold*	0.5% rated current (max)

*As defined by ARP 490

Resolver Specifications (Control and Slave)

Item	*Characteristics*
Primary voltage	7 volts
Frequency	1660 Hz
Current	0.010 amp
Power	0.015 watt
Impedance ZRO	128 plus J650
ZSO	28 plus J176
ZSS	23 plus J16
DC resistance (rotor)	56.8 ohms ± 10%
DC resistance	7.5 ohms ± 10%
Phase shift	5.6 deg
Range	75^{o}/1.5 in. stroke or 97.50 deg to 172.5 deg
Output voltage	3.5 volts

*This specification also applies to the RCVV actuator feedback resolvers

Table V-5. CENC Electrical Requirements

Electro-Hydraulic Servo Valve Specifications

Item	*Characteristics*
Rated current	± 20 ma
Max current	45 ma
Inductance	0.5 henries/coil at 50 Hz
Null bias	−6 ± 0.4 ma
Coil configuration	Two (2) independent coils
Coil resistance	160 ohms ± 10%
Threshold	<0.5% of rated current
Hysteresis	<4% of rated current

Resolver Specifications

Item	*Characteristics*
Primary voltage	7 volts
Primary frequency	1660 Hz
Input current	0.010 amp
Input power	0.015 watt
Impedance ZRO	128 plus J650
ZSO	28 plus J176
ZSS	23 plus J16
DC resistance (rotor)	56.8 ohms ± 10%
DC resistance	7.5 ohms ± 10%
Phase shift	5.6 deg
Output voltage	3.5 volts

SECTION VI
FADEC REQUIREMENTS

SECTION VI
FADEC REQUIREMENTS

A. GENERAL DESCRIPTION

The FADEC system, as configured for the INTERACT program, consists of two engine-mounted units that provide full authority digital electronic control of the F100 turbofan augmented engine from start through full augmentation. Each of the two units, designated as Primary and Secondary, is functionally equivalent and has identical control capability. The current FADEC system is shown schematically in figure VI-1. Digital communications between the primary and secondary units allows exchange of sensed and calculated information to provide extensive fault tolerance capability. Parameter synthesis provides for continued safe operation of the engine in the event that measurement capability is disabled. Separate dual windings are employed on electro-hydraulic interfaces, with each winding dedicated to one section of the controller. Output switching logic is employed such that only one processor commands a particular output at a given time, but individual outputs can automatically be transferred from primary to secondary command.

B. SYSTEM FEATURES

Comprehensive software and hardware features are incorporated to identify system malfunctions, implement redundancy management, and facilitate system maintenance. Should a malfunction occur which prevents engine control from the primary unit, the secondary unit outputs are automatically activated.

The paragraphs that follow provide a more detailed description of the current FADEC structure and a preliminary definition of changes/updates required for the INTERACT with FADEC program.

1. FADEC Fault Accommodation

FADEC employs dual-path redundancy to provide a highly fault-tolerant, fail-operational/fail-safe system concept. A simplified schematic of this concept is illustrated in figure VI-2. As shown in this figure, FADEC is divided into separate primary and secondary systems, each incorporating a digital processor and a complement of input and output circuitry to provide full authority digital electronic control of all engine and augmentor functions. Self-test and fault detection features are included to implement corrective action in the event of failures within the systems, external sensors, or output devices.

The Primary and Secondary processors communicate with each other in real time. Because of this communication capability, any failure of one system input parameter (which is made available to both systems by redundant sensors) may be accommodated because the same parameter is available through interrogation of the other system.

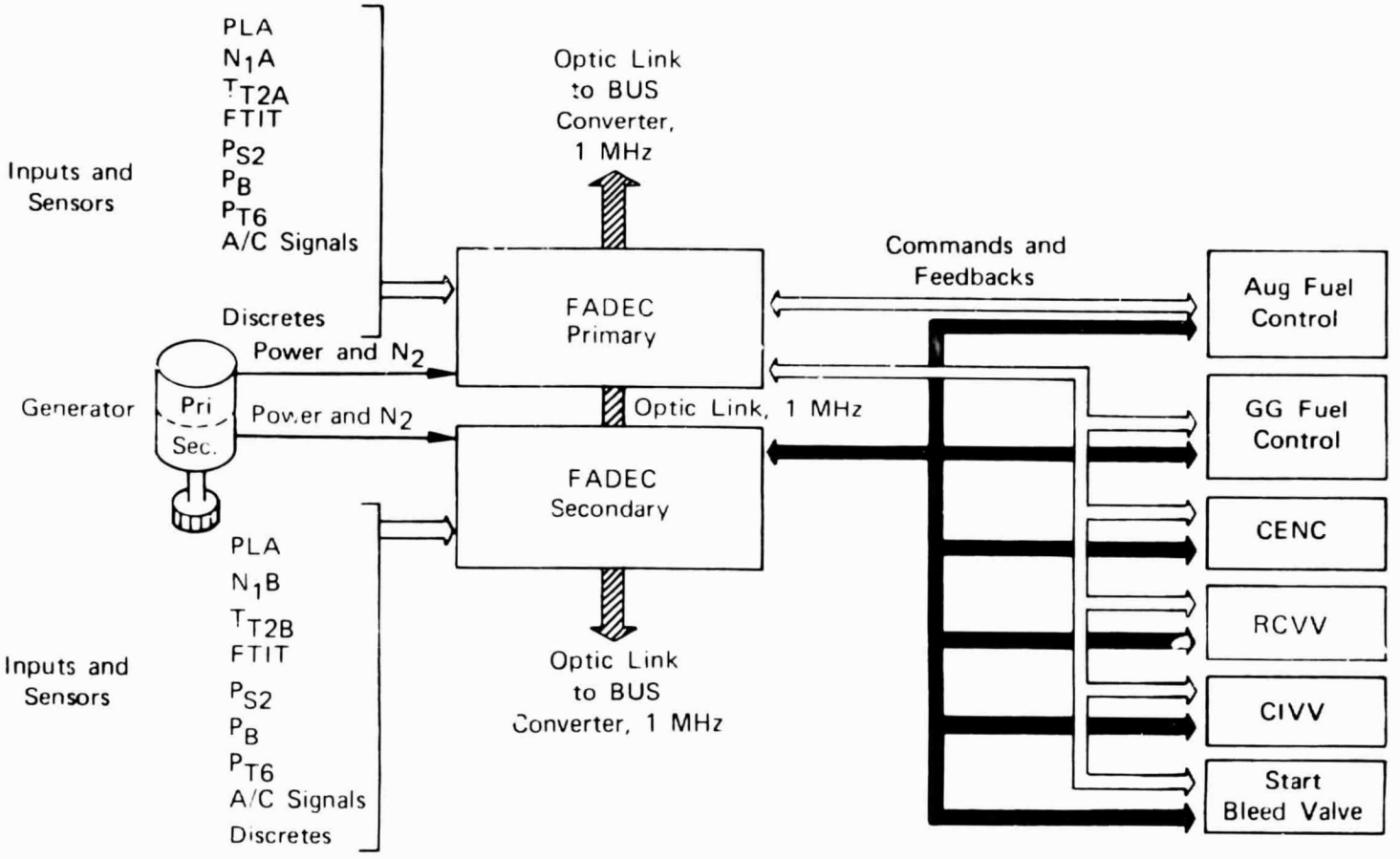


Figure VI-1. FADEC In INTERACT

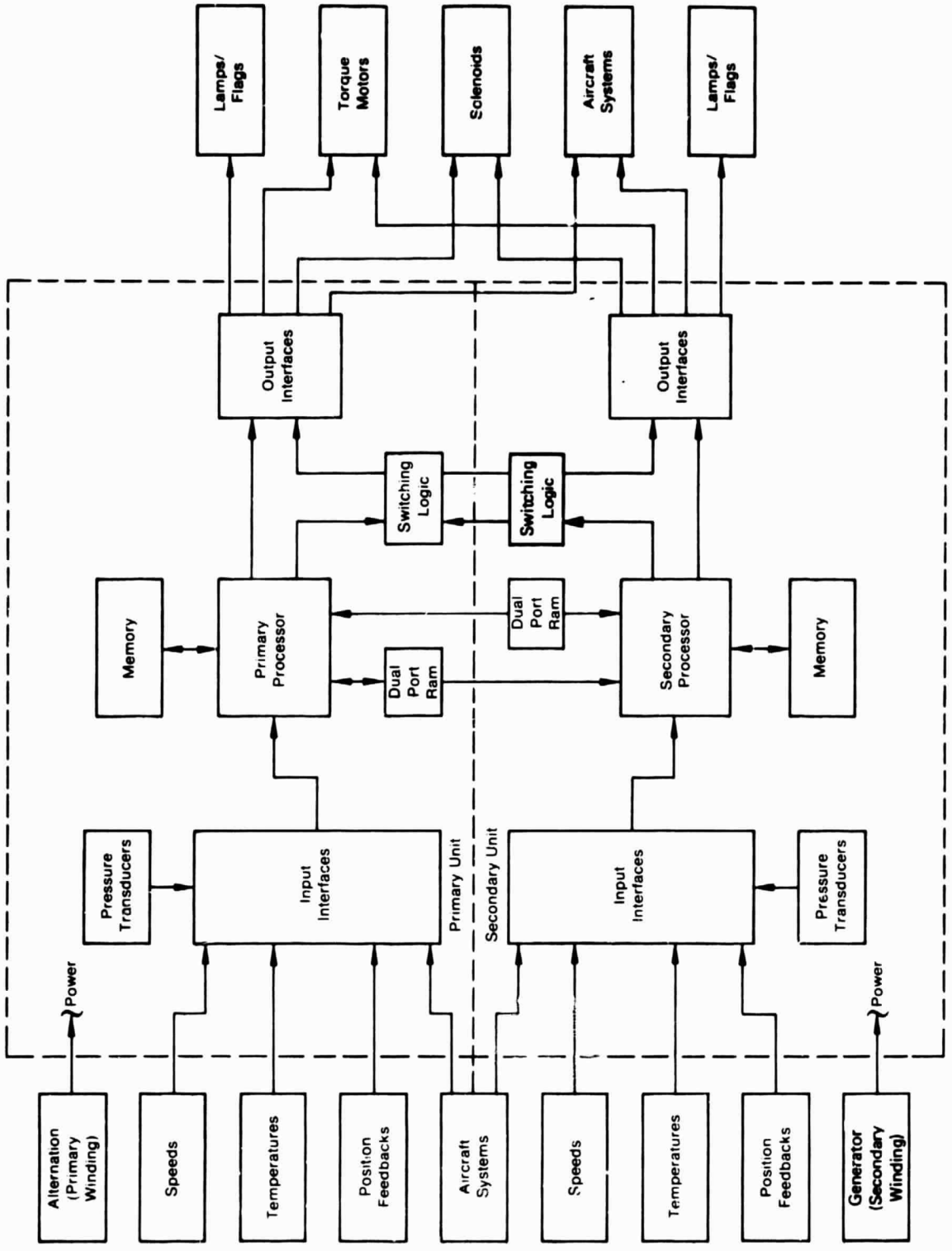


Figure VI-2. FADEC Electronic Unit Organization

Input/Output functions are provided by a complement of sensors and servo-actuators (effectors). These are comprised of thermocouples, resolvers, magnetic pickups, pressure sensors, torque motors, and solenoid valves. Communication between the digital processors is facilitated through the use of dual-port Random Access Memories (RAM). Each FADEC unit has a dedicated transmit and receive (32 words each) memory block whose data transfer between processors is controlled by a UART-driven 125K baud serial optic data link. This data transfer is asynchronous and program-transparent to each processor. This communication system allows input signals to be shared by the two processors, providing input signal redundancy. As an example, in figure VI-3a, if the rear compressor variable vane angle (RCVV) position feedback resolver malfunctions in the primary path, the primary will retrieve the RCVV actuator position signal from the secondary via the dual-port RAM. In addition to the signal sharing, some inputs are duplicated by means of parameter synthesis and used to identify input signal in range malfunctions.

It should be noted that provision is made not only for the capability to switch one system in to replace the other in the event of major malfunction, but individual output loops may also be switched in and out in the event of less significant malfunctions. Maximum flexibility is thus provided in response to any malfunction situation.

All output loops are checked on a continuous basis throughout the flight phase of engine operation by the loop continuity check. The past command error signal to each torque motor is compared with the present position of the output actuator to determine whether or not the proper direction of movement has taken place during the previous output update cycle. Once a fault is detected, a switchover to secondary control of the particular output loop in question is effected, as shown in figure VI-3b for the CIVV torque motor. Output effector loops are driven by their respective processors. There is no cross-coupling of output command signals from the primary processor to the secondary output drivers or vice versa.

As in the torque motor case, individual solenoid output states are fed back to the processor for comparison with desired solenoid states for fault detection. On engine start-up, all solenoids are read by the processor and compared with the prescribed limits to determine possible output driver/solenoid faults. If none are confirmed as faulty, operation continues with each solenoid being checked continuously and also when a state change is commanded by the processor. With a second reading being taken on a change of state, confirmation of faulty operation is possible. When a fault is confirmed, the solenoid driver is switched out, with the secondary backup driver being simultaneously switched in. This fault-checking mode allows fault differentiation to the FADEC or the solenoids themselves.

In addition to the previously described software tests, the FADEC also provides hardware tests. To protect the processor from being caught in an infinite loop, the computer cycle time test is performed. A computer cycle timer, or watchdog timer, is employed to monitor the update rate of the processor program. If the processor becomes caught in an infinite loop, the cycle timer will not be reset within the allotted time, resulting in a reset of the entire program and a switchover to secondary control.

A power supply test function is employed to monitor proper voltage regulation. A detected fault results in a switchover to secondary control. This hardware test signal is known as power supply reset (PSR) and goes to the switchover logic to effect a changeover to secondary control.

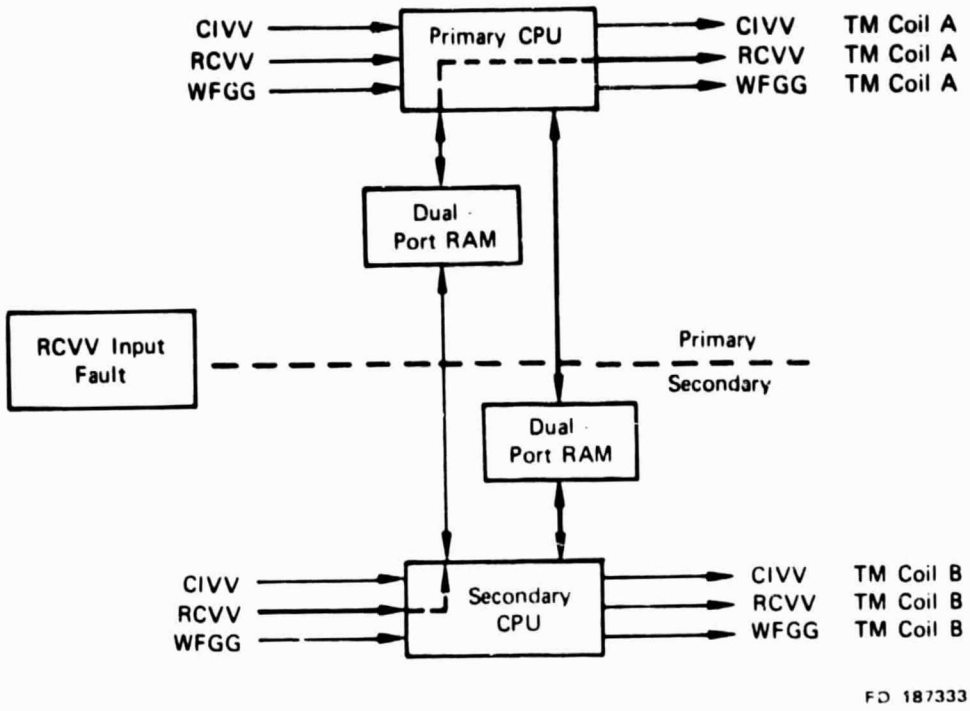


Figure VI-3a. FADEC Fault Tolerant Concept

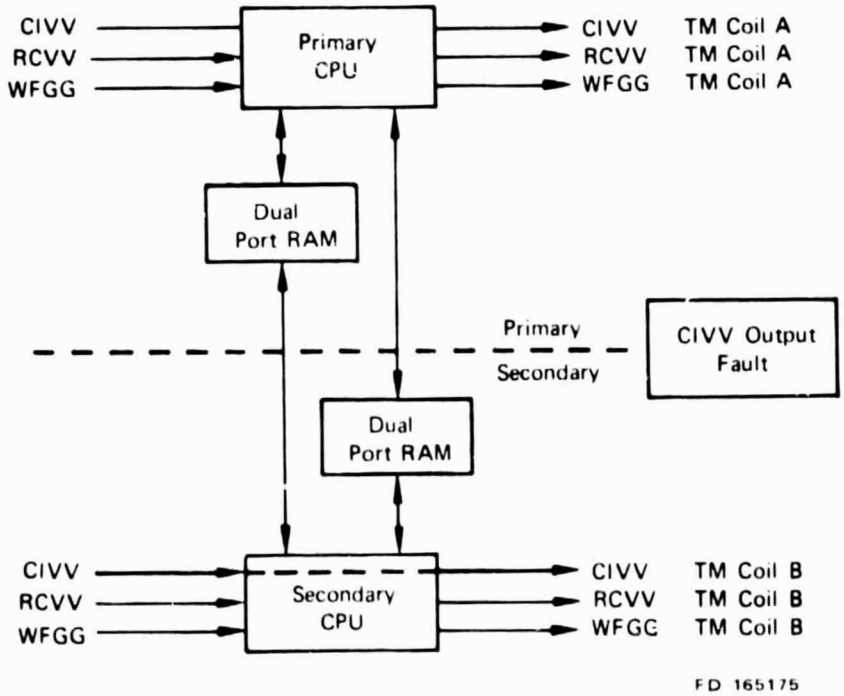


Figure VI-3b. FADEC Fault Tolerant Concept

2. CPU Implementation

The central processor unit (CPU) design is a proprietary design based on the Hamilton Standard HS 16/24 processor.

The HS 16/24 CPU is a flexible controls-oriented, CMOS LSI, bit parallel, fractionally scaled two's complement, combinational logic, solid-state machine. It was initially designed for either 16- or 24-bit word lengths (16 bits for fuel controls and 24 bits for navigational computations), and may be operated with supply voltages from 0 to +15 vdc, and temperatures from −55 to +125°C. It is structured with six dedicated registers, a program incrementer, an arithmetic logic unit (ALU), and hard-wired control logic and timing. The 87 instructions of the CPU are designed to operate with a microinstruction controlled clock which can synchronously vary the microinstruction execution times between 294 and 588 nsec and 1.176 μsec, allowing high-nsec speed instruction execution. Instruction execution times are also reduced via overlapped fetch/execute cycles, look-ahead carry in both the arithmetic unit and the register unit adders, and judicious selection of all register transfer paths for simultaneous multiple-register transfers.

The digital logic required to implement the CPU design was partitioned into four different, custom, large-scale integration (LSI) types. Five LSI devices and two standard CMOS SSI (small-scale integration) packages were used in the 16-bit processor design. These include the following:

- One Timing CMOS LSI Module
- One Control Logic A CMOS LSI Module
- One Control Logic B CMOS LSI Module
- Two eight-bit Register/ALU CMOS/SOS VLSI (Very Large Scale Integration) Modules
- Two CD40XX CMOS SSI Devices.

3. Primary/Secondary Switchover Circuit

In addition to the communication path provided by the dual-port RAM, four fault status discretes are transmitted from the Primary to the Secondary and vice versa. These discretes provide a hardwired backup information interchange system in the event that the RAM communication is disabled. These four discretes provide multiple states of fault information to the other processor so that individual output loop switchover can take place under a multifault condition. Since each system is capable of providing all the engine control functions, it is desirable that the decision as to which system is in control at a given time be validated by a third intelligence or voter, the so-called "Smart PROM." This circuitry receives input signals, or discretes, from each of the two controls, and based on a predefined state table, makes a decision as to which control is in the better health and should therefore be placed in command.

The switchover circuit is designed to disable one unit in the event of a failure. This circuit is highly reliable and designed to operate in the event of any single failure. As indicated in figure VI-2, the switchover circuitry will be located in both FADEC controls. Power is obtained from the primary and/or secondary supply, and a separate 10vdc supply created. The inputs into this control logic are clamped to prevent latch-up. The actual logic implements a CMOS PROM to replace discrete devices, which will simplify any modifications due to a change of system definition. The PROM controller will also reduce part count by eliminating several discrete devices, thus increasing overall reliability. The PROM outputs are open drain with pull-up resistors to the respective units to prevent latching up any logic. In the case where both outputs are somehow pulled low discrete logic in each unit will cause both enables to go high.

The PROM controller receives inputs from each of the two controls indicative of the following:

- Power Supply Health – PSR (Power Supply Reset)
- Pilot Intention – Enable (Pilot Discrete)
- System Health – System OK (Processor Discrete)
- Improper CPU Operation – Cycle Time Test (CTT)
- Processor Stoppage – Clock Loss (Clock Loss).

The voter determines, on the basis of the above discretes via a priority scheme, which of the two controls is most capable of achieving 100% operational performance. Under normal conditions, with both systems fault free the two outputs of the voter would be set to logic 0, allowing the Primary to control the engine with the Secondary acting as a backup. If both processors fail, control of the engine would be transferred to a hydromechanical computer located in the Gas Generator control.

4. Memory

The FADEC memory (figure VI-4) is comprised of four different memory subsystems:

- 12K-word by 16-bit PROM
- 384 words of RAM
- 64 words of CPU-alterable ROM (CPUAROM)
- 64 words of dual-port cross-talk RAM (DPCTRAM).

a. Programable Read-Only Memory

The programable read-only memory is the main-program read-only memory for the control and is specifically designed to:

- Minimize memory parts count and printed circuit board (PCB) area
- Reduce memory power dissipation
- Provide maximum development flexibility
- Access 256 words of PROM from each pressure sensor

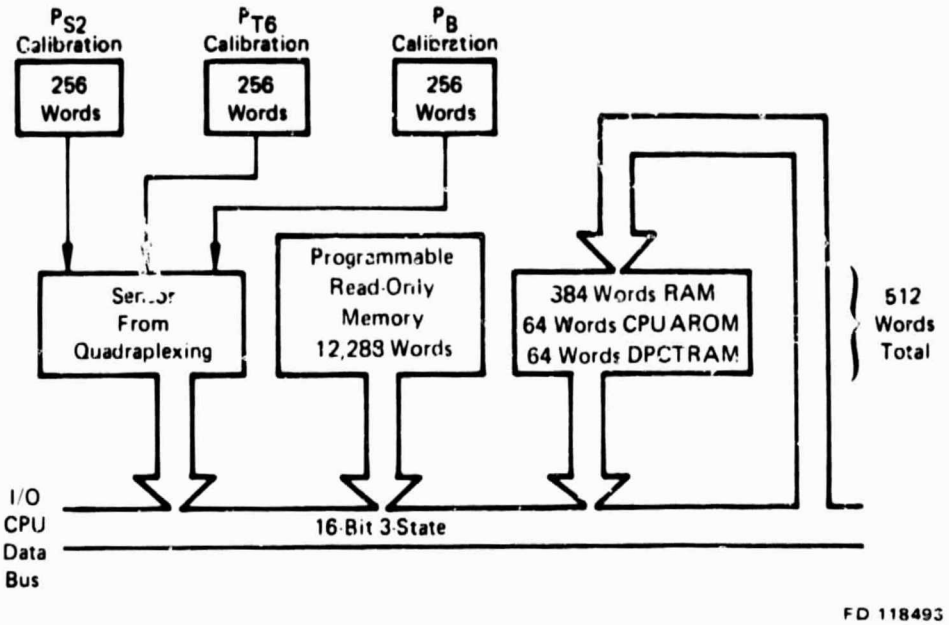


Figure VI-4. Memory Organization

Each 2K words of memory is made up of four 8K-bit integrated circuit (IC) packages. To allow maximum CPU execution speed, these four devices are accessed by the CPU in parallel; therefore, the four 4-bit devices make up 2048 X 16-bit words.

Pressure sensor calibration data, usually 32 words per absolute sensor plus 224 words of additional program memory, is available in each of three pressure sensor calibration PROM's. This memory is implemented with 1024 X 4 PROM IC's.

b. *Random Access Memory*

The random access memory scratch pad is specifically designed to: (1) provide up to 512 X 16-bit words of directly addressable (page zero) scratch pad memory for the CPU and (2) reduce power dissipation through the use of SOS/CMOS RAM IC's. The SOS/CMOS RAM IC's are accessed in parallel to allow maximum CPU execution speed.

c. *CPU-Alterable Read-Only Memory*

The CPU-alterable read-only memory is a single 42-pin hybrid flat-pack comprised of two 16-bit EAROMs and all the control logic required to interface with the CPU. This configuration allows only the CPU to alter memory, preventing improper external programing of the EAROM devices.

5. Input/Output Definition

The parameters, types, and ranges of inputs and outputs processed by the current FADEC are shown in table VI-1.

Inputs are fed into each central processor unit (CPU) via time-multiplexed digital converters (A/D), resolver-to-digital converts (R/D), and digital pulse counters. All of these interfaces are read into the CPU on a three-stage input/output (I/O) bus. CPU inputs are received as parallel 16-bit words.

Output signals from the processor are handled similarly, with commands being sent out serially, via the I/O bus, to the digital-to-analog converters (D/A). The D/A converts the digital word to a voltage level proportional to the magnitude of the command, providing control of the output drivers which power the effectors.

Also included are serial digital data I/O drivers. The serial digital data optical bus provides a means of communicating between the primary and secondary.

a. Engine Inputs to FADEC

(1) Pressure Inputs to FADEC

The P_B, P_{T6}, and P_{S2} pressure sensors are modular units for ease of installation and removal. The modules each consist of:

- Basic thin-walled vibrating cylinder assembly with integral spool body, drive and pickup coils, and temperature sensor
- Mounting base housing assembly with guide pins, captive hardware, and electrical I/O connector
- Electronic submodule containing the sensor's uniquely programed PROM and serving as an interconnection device between the electrical I/O connector and the PROM, drive and pickup coils, and temperature sensor.

Each sensor module is a completely interchangeable plug-in entity which provides its own unique calibration data, the PROM being an extension of the FADEC processor memory system. The sensor output is a CMOS compatible square wave with a frequency that is related to input pressure.

(2) Speed Frequency Inputs

Frequency or pulse-rate-type input signals are converted to digital words by use of one of four separate pulse-rate-to-digital converters. There are a total of five input signals which are converted by the four converters: N_{2A}, N_{1A}, T_{T6}, P_{S2}, P_B.

Table VI-1. Engine Sensor Parameters and Command Functions

Input Parameters			*Command Functions*	
Parameter	*Signal Type*	*Range*	*Parameter*	*Signal Type*
N1	Frequency	1,400 to 13,000 rpm 800 to 8,000 Hz	CIVV	Torque Motor
			RCVV	Torque Motor
N2	Frequency	1,300 to 15,000 rpm 1,800 to 19,000 Hz	CEXC	Torque Motor
			WFGG	Torque Motor
P_{S2}	Pressure	1.0 to 50 psia	WFAC	Torque Motor
P_B	Pressure	2.0 to 600 psia	WFAD	Torque Motor
P_{6M}	Pressure	2.0 to 110 psia	Seg Seq	Torque Motor
T_{T6}	°F	-65 to 440°F	Aug [illegible]	Solenoid
TTIT	°F	-65 to 2,000°F	Start Bleed	Solenoid
A_J	Resolver	3.1 to 7.2 ft^2 92.5 to 177.5 deg	Mode Select	Solenoid
CIVV	Resolver	-30 to -5 deg 92.5 to 177.5 deg		
RCVV	Resolver	+4 to -40 deg 92.5 to 177.5 deg		
PLA	Resolver	0 to +130 deg 92.5 to 177.5 deg		
WFGG	Resolver (2)	100 pph to 16,710 92.5 to 177.5 deg		
WFAC	Resolver	0 to 45,000 pph 92.5 to 177.5 deg		
WFAD	Resolver	0 to 45,000 pph 92.5 to 177.5 deg		
Seg Seq	Resolver	92.5 to 177.5 deg		
Quickfill	Discrete	<1Ω to >100kΩ		

(3) Resolver-to-Digital Converter

Angular shaft position is detected through the use of resolvers. Sixteen different resolver inputs (8 active resolver channels, 6 spare resolver channels, and two test signals) are multiplexed into one resolver-to-digital (R/D) converter through the use of a CMOS analog multiplexer. The address of the multiplexer is selected by the processor.

All resolvers on the EHMI, with the exception of the augmentor control and CENC, are dual and will be excited and F/B to the appropriate control separately. For the INTERACT program the augmentor resolver information and exhaust nozzle position from the CENC will be switched between primary and secondary control.

(4) Temperature Interface

The FADEC unit will contain two thermocouple inputs (FTIT and T_{T2} thermocouples). Thermocouple cold junction compensation is done in an isothermal block with a platinum resistance element. The platinum resistance probe is used for its predictable and repeatable characteristics. The linearity of this type of sensor reduces the burden of CPU curve fitting and allows for interchangeability without calibration.

(5) Discrete Input Interface

There are six external discretes (switch closure type) inputs. These inputs are buffered via a resistor, capacitor, and diode network. The buffered inputs are joined with internal discrete signals to form a parallel digital word. This word is multiplexed onto the processor input bus lines when it is properly addressed.

The input buffers are designed such that an open switch contact (greater than 20 kΩ resistance) will result in a logic "1" input and a closed switch contact (less than 100 Ω) will result in a logic "0" input.

b. Output Interface

All FADEC output interfaces are updated, or loaded, by the CPU serially via the CPU serial output. The FADEC incorporates five types of output interface circuits: torque motor drive, solenoid drive, flag drive, dc excitation, and resolver excitation.

(1) Torque Motor Output

The Torque Motor Output Interfaces are required to accept an 8-bit binary word (consisting of seven magnitude bits and one sign bit) from the processor. The interface circuitry then causes a current to flow through the associated torque motor. The magnitude of the current is proportional to the magnitude of the binary word received from the processor, and the direction of current flow is determined by the sign bit.

In addition to the software-controlled current described above, the interface will provide a fixed value of offset current through its associated torque motor, such that the total current through the torque motor is the sum of the fixed offset current and the software-controlled current.

After a binary word is received by the interface, the current through the torque motor caused by this word will continue until a new binary word is received by the interface. However, if there is a power supply reset, or a BIT failure, the D/A will be reset to a down-trim value and torque motor switch will be opened.

All of the EHMI components have dual-wound torque motors, one coil will be energized from Primary, the other from the Secondary. Only the computer in control will be energizing its coil at any given moment.

(2) Solenoid and Relay Outputs

There are three solenoid and one relay output drivers in the FADEC. All the drivers are schematically/electrically identical and are driven from internal ±15 vdc (30 vdc) power supplies.

Failure mode detection and protection has also been designed into the driver. This includes a diode to suppress the inductive back EMF and foldback to protect the transistor switch from load short circuits. In addition, two switches, the transistor and a power FET provide a dual independent ability to disable three solenoids. The remaining relays and solenoids will be controlled by an AND gate and a transistor. Series resistors provide the capability of detecting a failure. This detection signal when fed to the processor via a high level mux and the three slope A/D converters will also determine which driver/solenoid has faulted and whether three is a failure in the FADEC. An overload of the ±15 vdc busses will result in activation of the PSR and a subsequent transfer of control to the secondary system.

(3) Fault Buffer

The fault buffer is designed to provide a CPU health status check between the FADEC Primary and Secondary controls. Serial digital data from each CPU is processed and tested in the fault buffer circuitry of each control. In the event an error is detected, one or more fault flags are set.

Failures which result in the inability of the processor to maintain safe engine control result in the transfer of control to the Secondary processor.

(4) System Output Enable Registers

The output enable register is designed to enable/disable the system torque motors and solenoids, depending upon system status. The information is received from the serial data line and is shifted into the registers on the leading edge of the gated system clock whenever the output enable addressing indicates the appropriate address. When a "1" appears on the enable line, all of the registers are cleared to "0," disabling all torque motors and solenoids.

To illustrate the operation of the output enable registers, assume a failure occurred in the CIVV output loop at which time the Primary would recognize this condition and set the proper control bit in the Output Enable Register to logic "0," thereby disabling Primary CIVV while simultaneously enable Secondary CIVV. In this instance, overall control of the engine would remain with the Primary although the CIVV output loop would be controlled by the Secondary CPU. Failures which would cause major errors in outputs would also be detected and, in this case, a complete switchover to secondary would be mandated. The voter would reset the Primary Output Enable Register to logic "0," causing all outputs to be disabled, simultaneously enabling the redundant Secondary outputs.

The same would hold true in the event of major faults in the Secondary. It is possible, under certain multifault conditions, that both Primary and Secondary systems would be disabled and cause transfer to the hydromechanical backup control. The pilot may also disable either the Primary or the Secondary as his discretion if engine performance appears to be substandard and request a hydromechanical backup control.

5. FADEC Diagnostic Capability

The FADEC unit incorporates self-test and fault detection features which can identify which control system component requires replacement to correct a malfunction, and in many cases it can also identify the subassembly within the component which is the source of the problem. When a failure is detected, the failure information is stored in electrically alterable memory within the control as well as the aircraft mission computer. This information may be interrogated at a later time by connecting a suitcase-sized AGE test set via test connector to the control.

The control system also has three fault flags and two cockpit caution panel lights. Two of the flags are mounted on the FADEC unit and indicate confirmed failures. The third flag is mounted on the aircraft avionics status panel and will indicate the operational status of the entire engine fuel control system. The cockpit-mounted caution lights indicate whether the engine is being controlled by the primary or secondary control system.

C. FADEC SOFTWARE

The FADEC software will be a derivative of the existent FADEC software, including the control mode and the failure detection. Modifications will be made to accommodate new hardware for both the optic interface and some internal redesign expected in the conversion to the INTERACT configuration. These revisions will be limited to that required to function properly within the communications protocol set up between the Primary and the Secondary and those required to maintain the present FADEC control mode with the new internal hardware.

1. Basic Logic for FADEC in INTERACT

A full authority digital electronic engine control refers to a control system comprising a digital computer and hydromechanical components that work together to control a gas turbine engine. The digital computer controls the engine over its entire operating range.

The electronic section of the control does all computations, schedules engine set points, monitors engine parameters, provides action for sensor failures and controls:

- RCVV – Rear Compressor Variable Vanes
- CIVV – Fan Inlet Variable Vanes
- Gas generator fuel flow
- A/B sequencing valve
- A/B core and duct stream fuel flow
- Nozzle area – A_j
- Start bleeds
- Augmentor ignition.

The hydromechanical section of such a control system provides for augmentor fuel distribution, provides simple backup for electronics off operation, and employs servovalves that provide the muscle for the electronics. Functional requirements of the system are:

- Provide satisfactory engine starting capability on ground and air
- Control gas generator fuel flow from idle to max
- Direct engine match control
- Schedule variable geometry
- Schedule augmentor fuel flow
- Provide direct inlet/engine coordination
- Provide failure mode protection.

The RCVV's are scheduled with N1, N2 and T_{T2}, whereas start bleeds and CIVV's are scheduled using identical parameters as the current F100 engine control:

- CIVV's scheduled as a function of N1 and T_{T2}
- Start bleeds scheduled as a function of N2 and T_{T2}.

Engine operating limits are protected by reducing gas generator fuel flow as required to avoid exceeding N2, N1, FTIT and P_B limits.

2. Air Inlet Control Interface

A high speed data link between the FADEC Primary, Secondary, and AIC-12 air inlet controller will allow either FADEC processor to implement the AIC-12 functions. The complete requirements for the AIC-12 are defined in McDonnell Aircraft Company procurement specification PS68-870045, Rev. C. This system is shown in figure VI-5. Only one of the FADEC processors will transmit command signals to the AIC-12 and the determination of which FADEC processor is commanding will be accomplished using the same technique as the torque motors.

To implement the inlet control functions (figure VI-6), three input parameters are required by FADEC: free stream pressure ratio (static/total), free stream temperature, and angle of attack. The FADEC processor will then calculate 1st and 4th ramp reference positions and reference throat pressure ratio, for transmittal to the AIC.

Communication with the AIC-12 will occur via the data bus converter box shown in figure VI-5. The box converts the optic signals to and from the FADEC computers into an electrical format. How the AIC data interfaces with the converter box will be determined by the aircraft systems integration contractor. The timing requirements of data transmission to and from the AIC-12 are governed by the current AIC-12 logic and timing implementation. The current nominal AIC-12 program cycle time is 11.55 msec with all outputs updated with each cycle. Therefore, a complete cycle consisting of data transmission from the AIC-12 to the remote processor, logic execution within the remote processor, and data transmission from the remote processor to the AIC-12 must not exceed 11.55 msec.

D. FADEC IN INTERACT ADDITIONAL CHANGES

1. General Description

The system configuration of FADEC in INTERACT is shown schematically in figure VI-5. The FADEC dual-channel engine-mounted redundant architecture will be used. The following paragraphs define those proposed changes and/or additions to the current FADEC hardware/software.

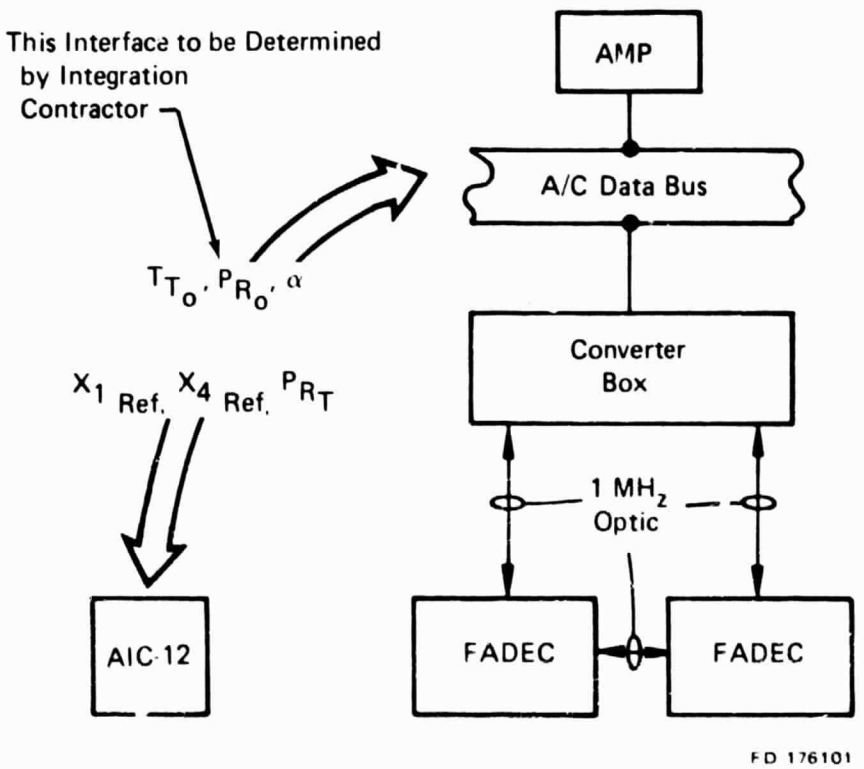


Figure VI-5 FADEC/AIC-12 Interface

2. Fault Accommodation

Dual path redundancy will be used in a manner that is functionally equivalent to the current FADEC. However the communications link between the FADEC units will be a 1 MHz optic channel. The data will be transferred between FADEC units under DMA (Direct Memory Access) control with no impact on program execution time.

Based on a strict piece part predicted failure rate per engine operating hour for mature hardware, the mean time between any single failure in the control system has been calculated to be 687 hours, for a dual FADEC flight configuration.

3. Memory

Provision for memory expansion will allow the following FADEC in INTERACT configuration:

- up to 16K words by 16-bit PROM
- up to 1K words by 16-bit RAM
- 128 words X 16-bit of CPU-alterable ROM

Allocation of the RAM (scratch pad) memory will be divided between the functions of:

1. Communications DMA memory
2. Page 0 directly accessable by all program logic
3. Local to each memory page directly accessible to the program logic within that page.

4. Optical Communications Data Links

Two high speed optic communication data links with a 1 MHz-bit rate will be provided in each of the two FADEC units. The format of the data word will allow a polling (controller to terminal) protocol. That is, the FADEC Primary will initiate/request data transfer to/from the Secondary.

A second high speed optic link in each FADEC Unit will provide communications with the Bus Converter. The format and protocol of this data link will be identical to that described above, and the data links within each FADEC unit will be implemented as multiplexed DMA channels.

5. Cockpit Indicator(s)

The cockpit indicator(s) will provide the pilot with a visual indication of the FADEC system status, of the built in test results from each FADEC unit, and of the control outputs.

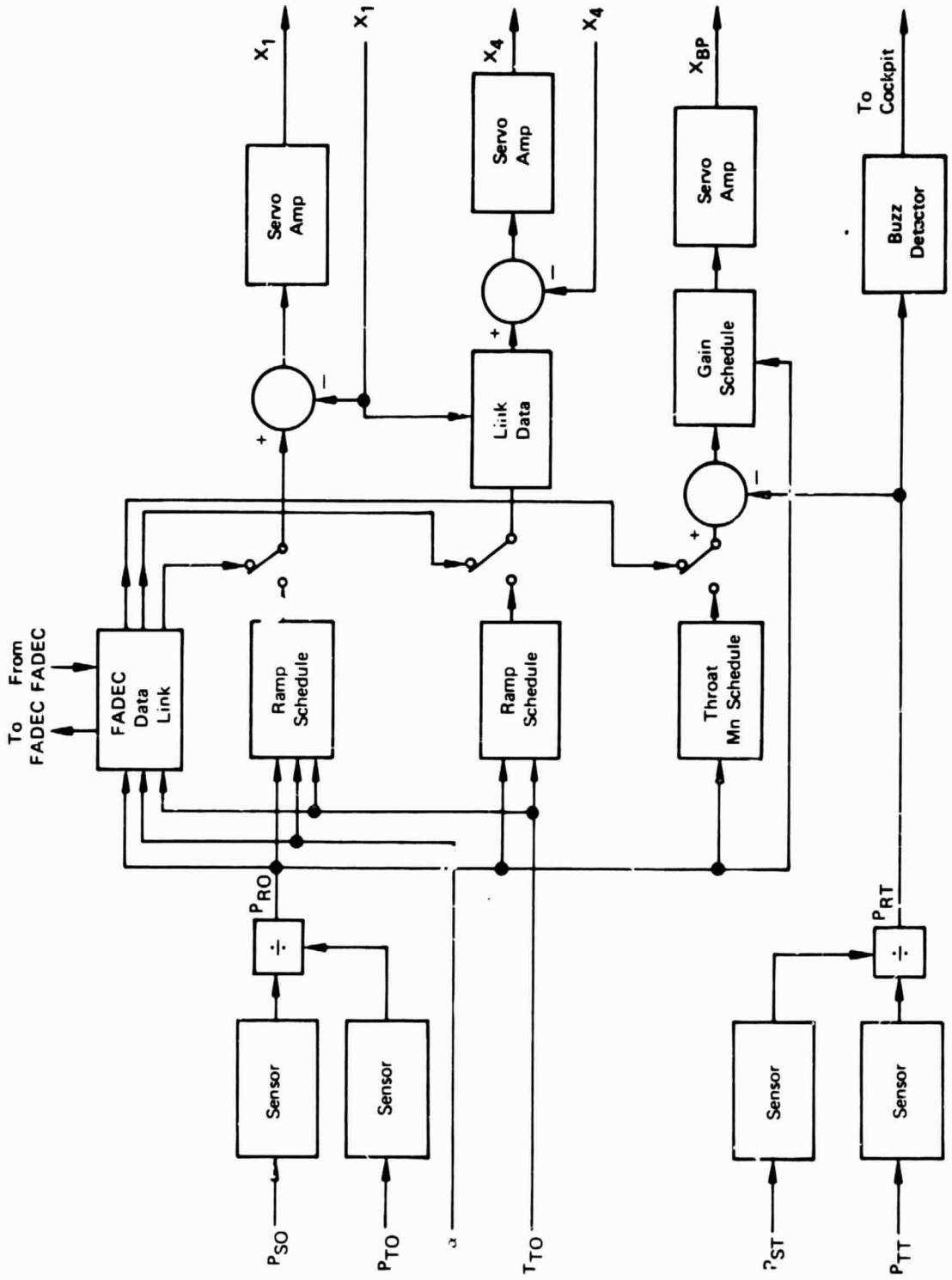


Figure VI-6. FADEC/AIC-12 Logic Diagram

SECTION VII
RPC REQUIREMENTS

SECTION VII
RESEARCH PROPULSION CONTROL (RPC) REQUIREMENTS

A. GENERAL

The Research Propulsion Control (RPC), as illustrated in figure VII-1, is an assemblage of hardware equipment and associated software programs which make up a digital electronic engine control. The RPC system will be used in conjunction with the EHMI to demonstrate advanced control approaches. Comprising the RPC system is a digital computer unit (DCU), an Interface Unit (IFU), and a Power Supply Unit (PSU). The RPC will be capable of controlling the engine from start through full augmentation.

1. Digital Computer Unit (HDC-601C)

The HDC-601 computer consists of a central processor unit (CPU), 32K X 16-bit core memory, power supply, 2.5 MHz crystal clock, and associated wiring, mounting, and cooling facilities. The CPU is constructed of TTL flat-pack circuitry mounted on 13 printed circuit (P/C) cards. The CPU is not packaged along functional lines; e.g., the A register is a part of the CPU P/C cards A1, A3, A5, and A7. The CPU contains timing and control, interface addressing (I/O and interrupt channels), direct-memory access (DMA), and arithmetic processing functions. The functional elements of the CPU are shown in table VII-1. Timing circuits provide signals to sequence data processing. Control circuits interpret commands and ensure that the required circuits are activated to accomplish a given processing operation. Interface circuits provide the capability to transfer computer compatible data to and from the external devices. Addressing circuits permit random access of memory and the means by which addresses can be altered. Arithmetic circuits, incorporating double precision capability, provide parallel processing of arithmetic functions in two's complement form. Eighty-four instructions are provided.

Table VII-1. Central Processor Functional Elements

A Register
B Register
Program Counter
Memory Address (Y) Register
External Priority Interrupt
External Interrupt Register
Discrete Decode Function
Instruction Decode
Timing
Direct Input/Output Channel (DIO)
Direct Memory Access Channel (DMA)
Adder
F Register (4 Bits of OP Code)
M Register
Shift Counter
Index Register
Interrupt Mask Register
Interrupt Control

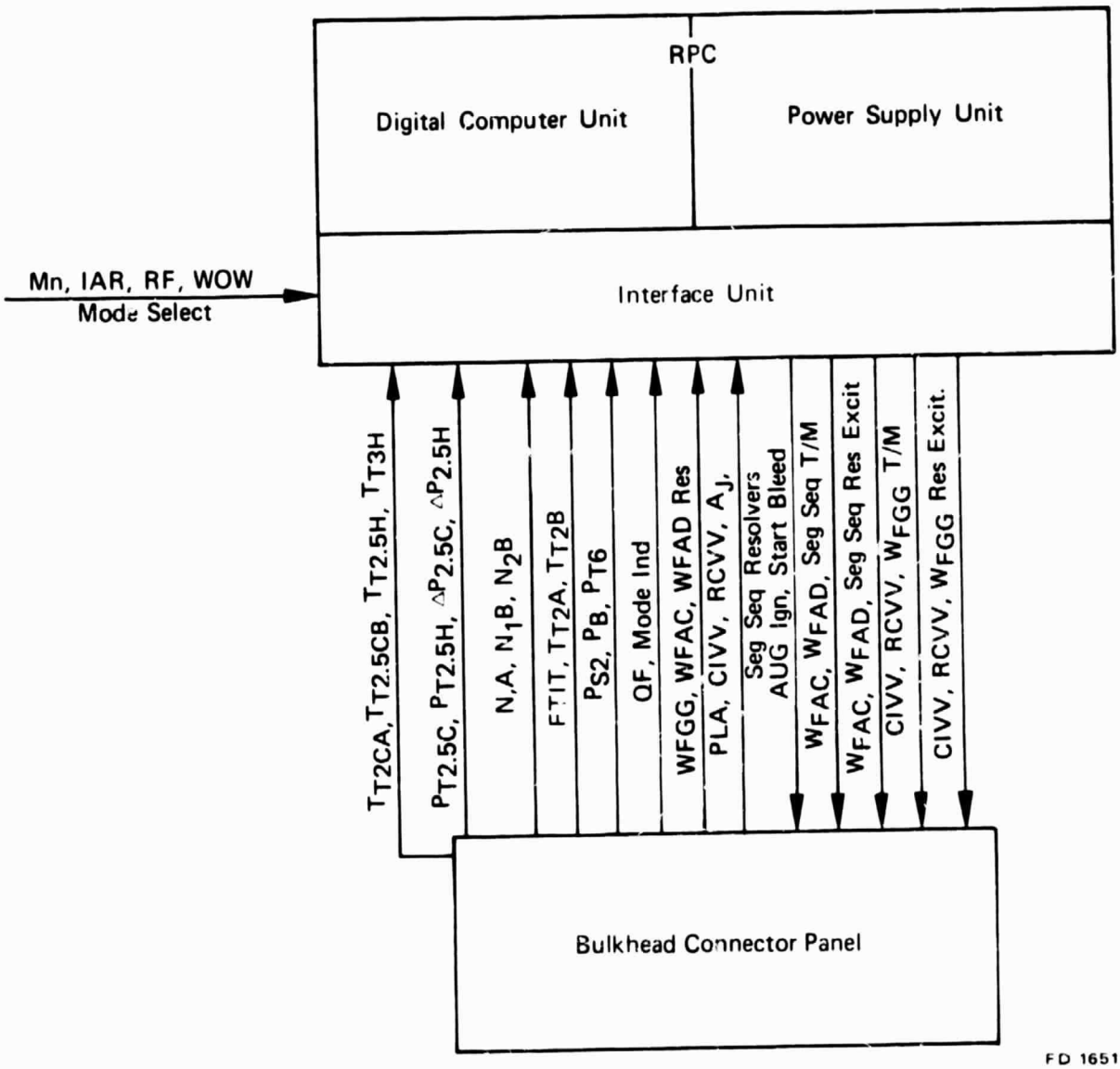


Figure VII-1. RPC to Engine Interface

2. Interface Unit (IFU)

The Interface Unit (IFU) interfaces the DCU to the system sensors, effectors, and test equipment. It conditions analog signals to digital signals for input to the DCU and converts digital signals from the DCU to analog outputs. Built-In-Test (BIT) features are incorporated into the IFU circuitry to provide an automatic monitoring hardware function.

The IFU can be described in terms of four basic blocks: (1) input electronics, (2) output electronics, (3) computer interface electronics, and (4) power supply electronics. Each of these functional blocks is illustrated in figure VII-2.

a. Input Electronics

The input electronics section provides capacity for 64 analog-to-digital (A/D) input channels. Two A/D converters run simultaneously. The 32-input high-level A/D digitizes analog signals within a ±5 vdc range; the 32-input (16 existing and 16 to be added for INTERACT) low-level A/D digitizes analog signals within a ±30 mvdc range. The least significant bit is approximately 15 μv for the low-level A/D. The conversion accuracy from IFU input to digital word is ±0.1% and the average conversion time is 105 μsec (two simultaneous conversions at 210 μsec each). Input filters will be modified to roll off the analog inputs at 20 Hz. All inputs are differential, with common mode voltage capability of ±5 vdc and common mode rejection ratios of 10,000 for low-level A/D conversion and 500 for high-level A/D conversion. Both A/D converters use automatic null correction circuitry to ensure operation to ±0.1% over the full temperature range.

The input electronics also provide conversion of 11 frequency inputs:

- Two rotor speed tachometers (N1/N2) to ±0.5% of full scale
- Eight special frequency to digital converters for pressure transducers to ±0.06% of full scale.

Resolver-to-digital converters are provided for eight inputs. These converters provide digital representations of actual positions to within ±0.5 deg.

Other input features provided are:

- Five demodulators for LVDT inputs with nominal accuracy of ±3.5% of input signal, much better than 2.5% accuracy is obtained by software techniques.
- Sixteen buffered input discrete lines.

b. Output Electronics

The output electronics provides 16D/A outputs of ±10.24 vdc with an accuracy of ±1% of full scale. The D/A converter uses a scratch pad memory and control logic for automatic refreshing of outputs (engage solenoids, bleeds, etc.).

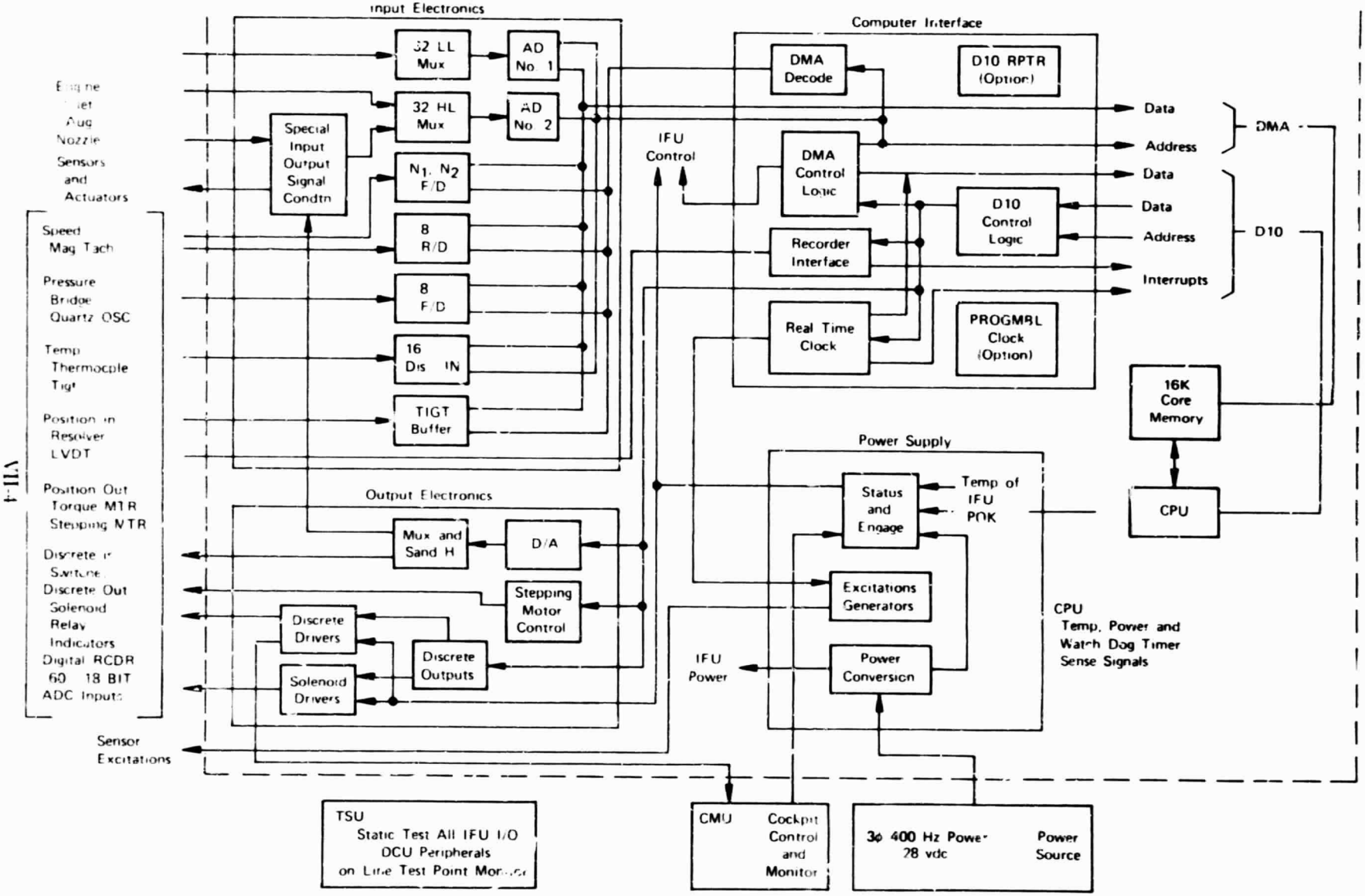


Figure VII-2. IFU Interface Functional Diagram

c. *Computer Interface Electronics*

This section provides transfer of data from the input electronics to the DCU via the direct memory access (DMA) bus. The DMA and DMA controller will require extensive modification to accommodate the added inputs. It also provides data to the output electronics by way of the Direct Input/Output (DIO) bus. In addition, the DIO bus is used for inputing data from the IFU DMA control circuitry and the IFU real-time clock. This circuitry consists of DMA control logic, DIO control logic, DMA bus driver, DMA decoder, and a real-time clock. A programable clock will be added for system reconfiguration. The DMA controller has some design features that prevent "lockup" of memory interface; the DMA access is limited to alternate DMA cycles, and a conversion timer prevents hardware failures from causing lockup of memory access. The DMA can address zone zero only.

d. *Power Supply Electronics*

Power supply electronics in the IFU provide precision excitation sources and system power up/down, engage/disengage control. Excitation generators of +5.0 vdc, −5.0 vdc, 5.0 madc constant current, 9.0 vrms at 1 kHz, and 9.0 vrms at 3.9 kHz are provided. Analog-to-digital conversions of these excitations, demodulated where necessary, provide capability for software corrections and ratio conversions of input signals, enhancing system accuracy without requiring high-precision excitation sources.

The status and engage logic provides hardware control over power up/down and control system engage/disengage. It automatically controls the system by sequencing power ON/OFF and ENGAGE/DISENGAGE, while monitoring various built-in-test (BIT) circuits to provide failsafe system control.

3. Power Supply Unit (PSU)

The power supply unit provides power for the IFU. The power input to this unit is 400 Hz, 3-phase and 28 vdc aircraft power.

B. RPC SYSTEM INPUT/OUTPUT

The RPC in its role as a propulsion controller is required to handle inputs from the engine sensors, resolvers, and discretes. Outputs consist of torque motor and solenoid power. The RPC will also process serial digital data from the aircraft data system. Tables VII-2 and VII-3 present the parameters required for BOM F100 engine control.

C-2

Table VII-2. IFU Inputs for Engine Control

Variable	*Nomenclature*	*Source*	*Remarks*
N1	Low Rotor Speed	BOM	
N2	High Rotor Speed	Alt (Engine)	Isolation Required
P_{T6}	Aug Duct Press. (Total)	P-Sensor Box	
P_B	Burner Pressure	P-Sensor Box	
T_2	Fan Inlet Temp	BOM	CH/AL
FTIT	Fan Turbine Inlet Temp	BOM (EHR)	CH/AL
Mn	Mach Number Data	1553 Data bus	Digital Word
IAR/Vmax	Idle Area Reset/Vmax	Airframe	Switch
RF	Rocket Fire	Airframe	Momentary Switch
WOW	Weight on Wheels	Airframe	Switch
Mode Select	RPC	Airframe	Switch
Mo	Mach Number Clock	Airframe	Frequency Signal
$T_{T2.5}$	Fan Exit Temp	Engine	CH/AL
CMV	Core Metering Valve	Aug Control	Resolver
DMV	Duct Metering Valve	Aug Control	Resolver
Seq. Valve Pos.	Segment Seq Valve	Aug Control	Resolver
QF	Quick Fill Signal	Aug Control	Switch
A_j	Exhaust Noz Area	CENC	Resolver
Optics	Optical Data Link	FADEC	
CIVV	Comp Inlet Variable Vanes	CIVV Act.	Slave Act. Resolver
RCVV	Rear Comp Variable Vanes	RCVV Act.	RCVV Act. 2 Resolver
PLA	Power Lever Angle	GG Control	Resolver
GG Wf	Gas Gen Fuel Flow	GG Control	Resolver
Mode	Pri or Backup Hydro	GG Control	Switch
P_{S2} Diag.	Inlet Press. Diagnostic	GG Control	Switch
T_{T2} Diag.	Inlet Temp Diagnostic	GG Control	Switch
T_{T3} H $P_{T2.5C}$ $P_{\ddagger}$ $P_{T2.5H}$ $\Delta P_{2.5C}$ $\Delta P_{2.5H}$ P_{S2}	Control Research Signals		

Table VII-3. IFU Outputs for Engine Control

Variable	*Nomenclature*	*Termination*	*Remarks*
Aug Ign	Augmentor Ignition	Aug Control	Solenoid
CMVR	Core Meter V lv Request	Aug Control	Torque Motor
DMVR	Duct Meter V lv Request	Aug Control	Torque Motor
Seq V lv Request	Seq Sequence V lv Request	Aug Control	Torque Motor
AJR	Exh Nozzle Area Request	CENC	Torque Motor
CIVV	CIVV Request	CIVV Master	Torque Motor
RCVVR	RCVV Request	GG Control	Torque Motor
St Bleed	Compressor Bleed	GG Control	Solenoid
GGMV	Gas Gen Meter V lv Request	GControl	Torque Motor
Aug Fault	Augmentor Fault	Airframe	Switch
RPC Fault	Res Prop Control Fault	Airframe	Switch

C. RPC SOFTWARE

Software for the RPC will be of highly modular design to accomodate varying control mode requirements. A strict structure will be set up for handling all hardware system functions such that the control algorithm will be insulated from all hardware dependencies and communicate only through data bases created and maintained by a host program. The host program will provide all timing and maintain the structure of the system by controlling the execution of all I/O modules. Research software should be able to be written with no impact on the host program so long as all common system services are provided in the original host design. Typical modules contained within the host to provide the hardware independence are:

1. Analog input
2. Servo loop control
3. Electrical MIL-1553B protocol
4. Processor self test
5. I/O self test
6. Power fail interrupt
7. Power up interrupt
8. Inter-task communication
9. Processor to processor communication
10. Control logic

To facilitate rapid development of reserach software, several functions frequently used by control algorithms will also be provided as system services. A typical, but not complete list includes:

1. Univariate curve read
2. Bivariate curve read
3. Filter
4. Lead lag compensation
5. Dead band
6. Hysteresis
7. Rate limit
8. Range limits
9. Double precision integrator

SECTION VIII
DEVELOPMENT PLAN

SECTION VIII
DEVELOPMENT PLAN

The recommended INTERACT with FADEC Development Plan, illustrated in figure VIII-1, is structured to maximize the amount of system verification prior to the start of flight testing. It is anticipated that changes to this plan will result from continuing discussions with NAPC, NASA, and the INTERACT Integration Contractor. Each major activity illustrated in the plan is described in the following paragraphs.

A. ELECTRO-HYDROMECHANICAL INTERFACES (EHMI)

Pratt & Whitney Aircraft is currently under a NASA contract (NAS4-2670) to provide electro-hydromechanical interface hardware and associated engine plumbing for the INTERACT Program. The interfaces are the same flight quality hardware that will be utilized in an electronic control demonstration and development program at GPD and as such, the hardware tests for flight suitability, reliability, and maintainability are considered as adequate for the NASA Program.

Following fabrication by the control system vendor, each component will be subjected to an acceptance bench test established by the vendor to determine that each unit will meet the functional requirements of the appropriate purchase specification, and verify all the performance characteristics specified. The vendor will also maintain records of all the acceptance test data for each unit procured.

Bench tests of all vendor items at GPD are required to provide continuity between subcontractor bench tests and the GPD closed loop bench tests which will be conducted under the NASA INTERACT Program. The tests provide an opportunity to ensure that a component is operating properly before testing it as a portion of a complex engine control system. Open loop tests in accordance with P&WA Component Test Schedules (CTS) established for each unit, will demonstrate the acceptability of each specific component.

Two complete sets of interface and associated engine plumbing are being procured. The hardware will be available for closed loop bench testing of the FADEC and RPC control systems as indicated in development plan. Expendable spare parts and essential electrical items required to support the use of this hardware are also covered under the NASA procurement.

B. FADEC

The recommended approach for continued FADEC development is to use the INTERACT aircraft as a vehicle to flight demonstrate FADEC. A significant ingredient of the FADEC/INTERACT association is to establish high-speed optical communication between the FADEC system and the aircraft. In addition, FADEC will demonstrate control of the aircraft inlet geometry, and fail/operational capability throughout the engine power range. These objectives will impose both hardware and software changes to the current FADEC system. To provide the necessary development flexibility, extensive use of breadboard FADEC computer systems both at the vendor and PWA/GPD will enhance optimization of the software development cycle and preliminary system integration tests on the closed loop bench. The breadboard systems also provide flexibility during both sea level and altitude

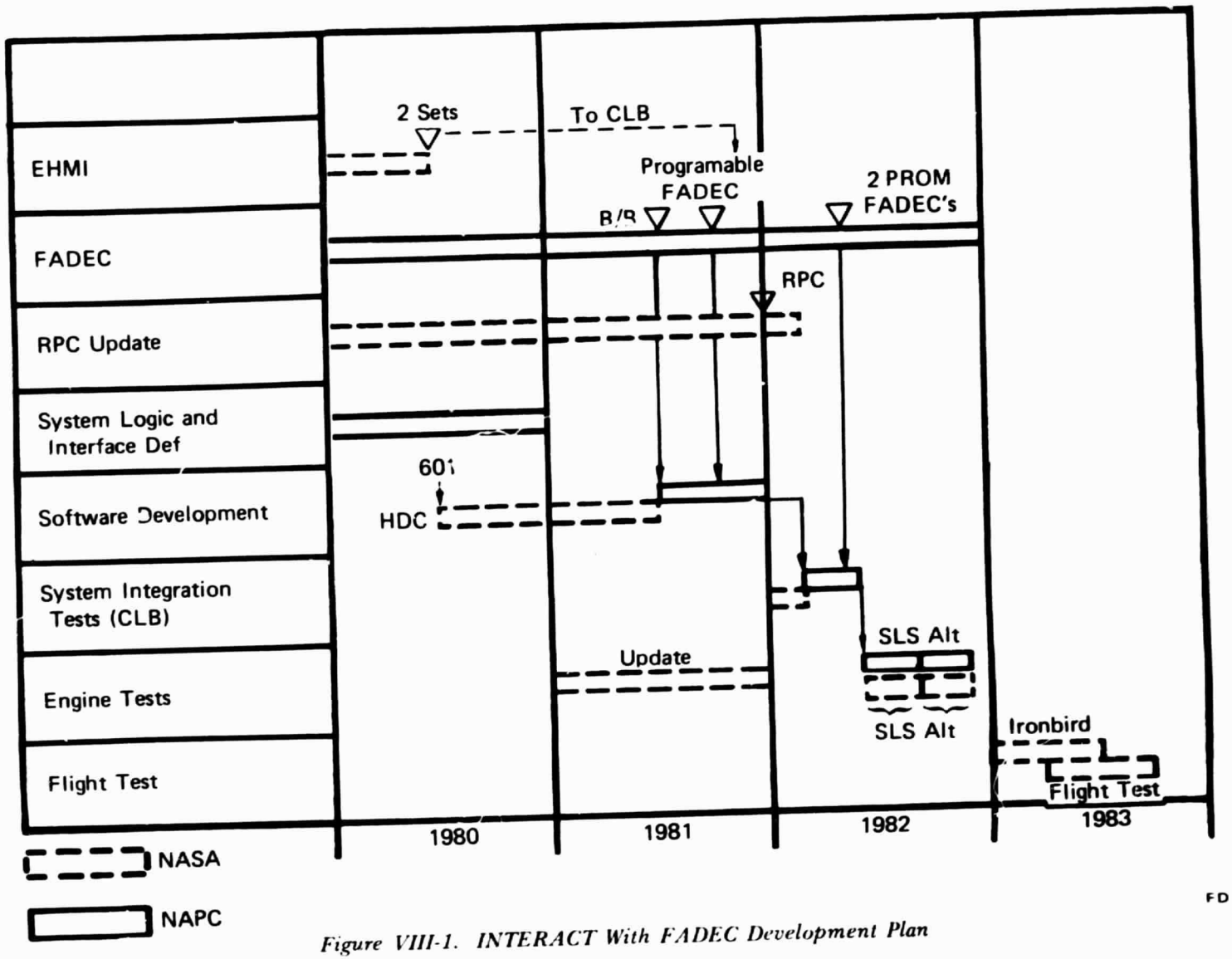


Figure VIII-1. INTERACT With FADEC Development Plan

engine testing. Further development flexibility is afforded through the use of a programmable FADEC computer that will be tested in conjunction with the FADEC breadboard. This dual computer configuration will conclude the software development phase and provide the necessary system checkout prior to system integration tests. The FADEC units delivered to NASA for flight will incorporate updated PROM's that result from extensive bench and engine testing. All testing accomplished during the FADEC activity will be coordinated with NASA to meet NASA requirements for safety of flight.

C. RPC UPDATE

In addition to reprogramming the Research Propulsion Control Computer with Bill-of-Material F100 control logic and unique logic developed for the INTERACT Program, the RPC will require hardware update to properly interface with the EHMI and the necessary complement of engine sensors. Some repackaging may also be necessary to meet aircraft installation requirements. Alternate means of interfacing with the EHMI should be considered during the initial phase of the INTERACT Program. Rather than modifying the existing RPC Interface Unit (IFU), closure of the servo loops and I/O signal conditioning could occur in an engine-mounted unit.

Concurrent with the RPC update will be development of the RPC system test set described in Section IX-C. It is likely two test sets will be built (modified), one as part of the NASA-DFRC simulation facility to provide software development and one to support system testing.

D. SYSTEM LOGIC AND INTERFACE DEFINITION

Logic development will encompass two major areas, FADEC modification and RPC system requirements. Meeting the Navy flight test objectives will require that new and/or updated system logic be generated to ensure full fail/operational capability throughout the engine power range, processor compatability with the high speed data link, and control of the aircraft air inlet geometry. A completely new software package will be necessary for the Research Propulsion Control. New executive software will be required to properly interface the RPC with the INTERACT system elements, and new engine control logic will be defined for development testing following the FADEC flight test phase. It is anticipated that initial RPC system testing will be implemented with multivariable control logic. Extensive use of dynamic computer simulations will facilitate initial development of the RPC system logic and minimize the amount of debugging prior to system testing. In addition to overall logic definition, RPC system interface requirements will be defined relative to sensor accuracies, effector rates, and data transmission. Comprehensive simulation tasks will again facilitate this activity.

E. SOFTWARE DEVELOPMENT

To maximize the efficiency of system bench testing it is imperative that software be fully exercised prior to the start of system integration testing. Use of the FADEC breadboard and test set unit (verifier) and associated peripheral equipment will enable complete checkout of the FADEC system software (executive routines, F100 engine control logic, fault detection/accommodation logic, and air inlet control integration logic). The same techniques will be utilized for the RPC system. The breadboard systems provide the flexibility to incorporate rapid changes to the software and checkout of those changes. In some

instances a simple linear model of the F100 engine can be used to evaluate changes in the FADEC and RPC system software. Also during this period, a comprehensive system integration test plan will be written that documents the test configuration, method of test, test objectives, testing sequence, and data acquisition/reduction.

F. SYSTEM INTEGRATION TESTING

The objective of bench testing is to verify proper operation of the control hardware and software with the entire system functioning together. The closed loop bench, described in Section IX-D, provides the means to verify system operation in real time utilizing a fully non-linear dynamic simulation of the engine and inlet process. The control system components are mounted as they would be on an actual engine (except for breadboard electronic controls). All pneumatic and hydraulic lines are the Bill-of-Material configuration. The simulations and control system can be exercised over the entire engine operating envelope thereby ensuring all I/O interfaces are working properly. The fault detection/accommodation logic can be checked by introducing actual or simulated faults in the system hardware. The closed loop bench tests will also demonstrate the functional suitability, response, and accuracy of the FADEC and RPC systems prior to committing the hardware to an actual engine test.

The FADEC and RPC systems will be run back-to-back on the bench. Final system software changes, defined during the test programs, will be implemented in the control computers, and a detailed sea level and altitude engine test plan will be developed during this time period. Sufficient bench utilization time should also be allotted to develop optimum use of GFE and maintenance procedures to be followed during the flight test program.

G. ENGINE TESTS

FADEC and RPC control system operation will be demonstrated at both sea level and altitude test conditions, over a period of approximately six months. Sea level testing will occur at PWA/GPD and altitude testing will be conducted at the NASA-Lewis test facility. The basic purpose of the engine test program is to demonstrate functional suitability of the FADEC and RPC control systems under actual engine operating conditions.

Basic tests to be conducted at sea level will include full modulation and checkout of all control loops, at least 50 hr AMT-type testing (engine cycles to be experienced during the complete flight test program), and distortion tolerance checks. These tests will provide the necessary system verification under conditions where the engine operation is well understood.

At altitude, additional functional checks will be run, but more emphasis will be placed on system stability/distortion testing and demonstration of stall recovery techniques. The test data accumulated during both sea level and altitude testing will provide sufficient data to not only evaluate engine performance but also determine final software changes necessary for the flight test program.

The engine test program described above applies to both the FADEC system and the RPC control configuration. It is anticipated that approximately 135 hr of actual engine test time will accrue during the test program.

H. FLIGHT TESTS

Prior to the beginning of flight testing the INTERACT system will be completely checked in the "ironbird." All subsystems, interface wiring/plumbing, software, and GFE can be evaluated in the actual aircraft installation configuration. Specific development activities relating to the FADEC and RPC systems are not clearly defined. Integration of the RPC with other aircraft systems (AMP, AIC, Data Link) must be demonstrated. The FADEC system must be capable of properly interfacing with the aircraft data system (converter box, down link, AIC). The ironbird will also allow demonstration of change over from the FADEC to RPC configuration.

Following the ironbird phase, the flight test program will be structured to demonstrate the Navy flight test objectives prior to reconfiguring the aircraft for the RPC system.

SECTION IX
SYSTEM TEST EQUIPMENT

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SYSTEM TEST EQUIPMENT

The major pieces of System Test Equipment required for the INTERACT with FADEC program are:

- Bendix Test Set
- FADEC Verifier
- RPC Ground Support Equipment
- PWA Control System Development/Integration Facility.

This equipment will be used during various phases of the program for verification, calibration, and troubleshooting of the INTERACT with FADEC hardware, software and logic. The units listed above are discussed in more detail in the following pages.

A. ELECTROHYDROMECHANICAL INTERFACE TEST EQUIPMENT

The Bendix electrohydromechanical interface (EHMI) units (gas generator control, augmentor control, CENC, CIVV, and RCVV) will be tested at PWA using a Bendix Test Set.

The Test Set positions all metering valves and actuators by controlling the servo valve torque motors. Closed loop feedback is provided by resolvers coupled to each servo valve. Manual command of position is accomplished by controls on the front panel of the Test Set, see figure IX-1. The Test Set provides a choice of either linear or step commands.

Each subsystem undergoing test uses its own set of controls and indicators, and each has individual cables for connecting into the proper test circuits. Thus, any number or all subsystems may be tested simultaneously.

An External Instrumentation connector provides simultaneous connections for input control signals to seven torque motor channels and for monitoring or recording seven torque motor currents and eight resolver angle positions. An Auxiliary Resolver connector allows input from an external resolver standard to any one of the eight resolver channels for calibration or special test purposes.

The Test Set will be used on the PWA flow test benches for checkout and calibration of the EHMI prior to Closed Loop Bench tests and troubleshooting any problems that might arise on the units.

B. FADEC VERIFIER

The verifier simulates the inputs and outputs to the FADEC control unit. The verifier will be used for check-out and testing of the FADEC unit during open and closed loop bench tests. For operational troubleshooting during the flight program, it will be used as the laboratory source for the FADEC I/O. The principal actions of the verifier are simulating the frequency, temperature, resolver feedback, torque motor, and solenoids within the system. Figure IX-2 shows a sketch of the verifier as currently configured.

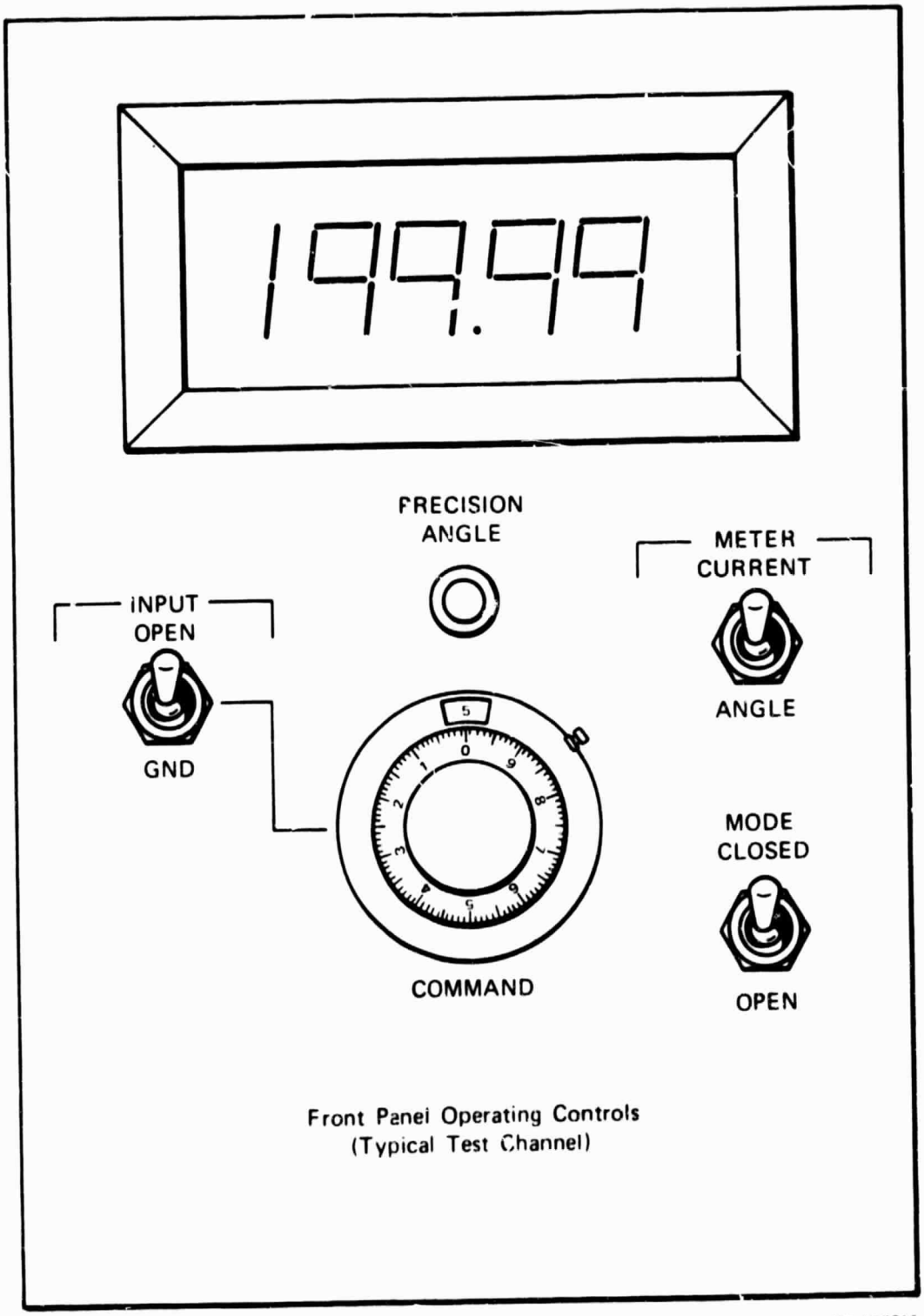

Figure IX-1. Bendix Test Set Console

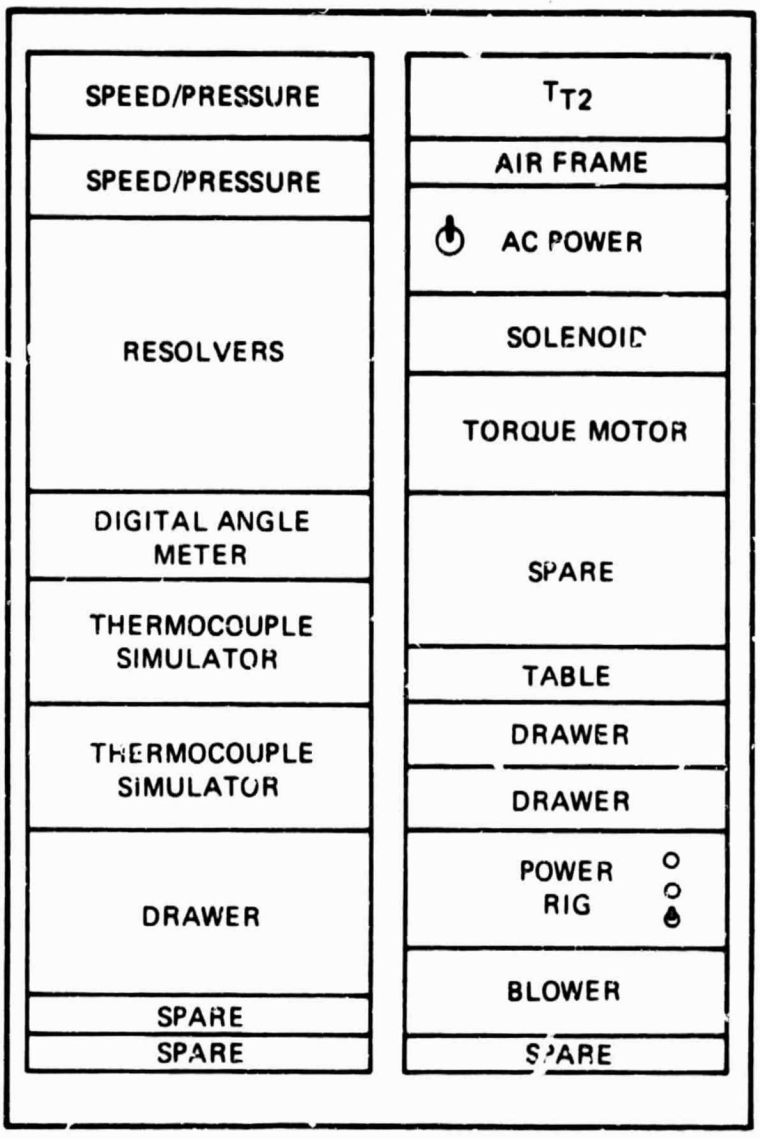

Figure IX-2. FADEC Verifier

The resolver feedbacks are provided by 14 resolvers (including spares) which are mounted with an angle indicator on the front panel. The redundant channels have a single resolver signal route to the FADEC control with the capability of injecting one of the spares into the system for simulating faults. A resolver angle indicator is provided for more accurate measurements of resolver position than provided with resolver dials.

The temperature signals are simulated by decade resistances.

The ten frequency sources simulate the low rotor speed (N1), high rotor speed (N2), and two spares, as well as the outputs of the vibrating cylinder pressure transducers for the pressure signals.

The spare frequency sources are used to simulate faults in a manner similar to that of the spare resolvers. A frequency counter is also provided for an accurate measurement of the function generator output signal.

The torque motors are simulated by resistive loads and have a current meter for each coil of each torque motor. There are a total of 24 meters, with one digital voltmeter provided for more accurate measurements when required.

The solenoids are simulated by discrete lights. Discrete inputs are simulated by panel mounted switches.

C. RESEARCH PROPULSION CONTROL GROUND SUPPORT EQUIPMENT (GSE)

The RPC GSE shown in figure IX-3 consists of the ASR-35 Teletypewriter (TTY), the Test Set Unit (TSU), associated software, and interconnections. A brief description of these elements is presented below.

1. ASR-35 Teletype

The ASR-35 teletypewriter prints data from the computer or transmits data to the computer via the keyboard. In the local mode, the unit can be used for off-line paper tape preparation, reproduction, or listing.

2. Test Set Unit (TSU)

The TSU is a portable test set designed to support the operation of the RPC digital controller. The TSU with the proper cable sets will allow checkout from RPC laboratory acceptance-type tests to direct GSE support on the flight line.

This unit may be used in two ways. First, it can be used to check out the IFU and the computer when these units are completely disconnected from the installation. Second, individual transducer signals may be statically displayed.

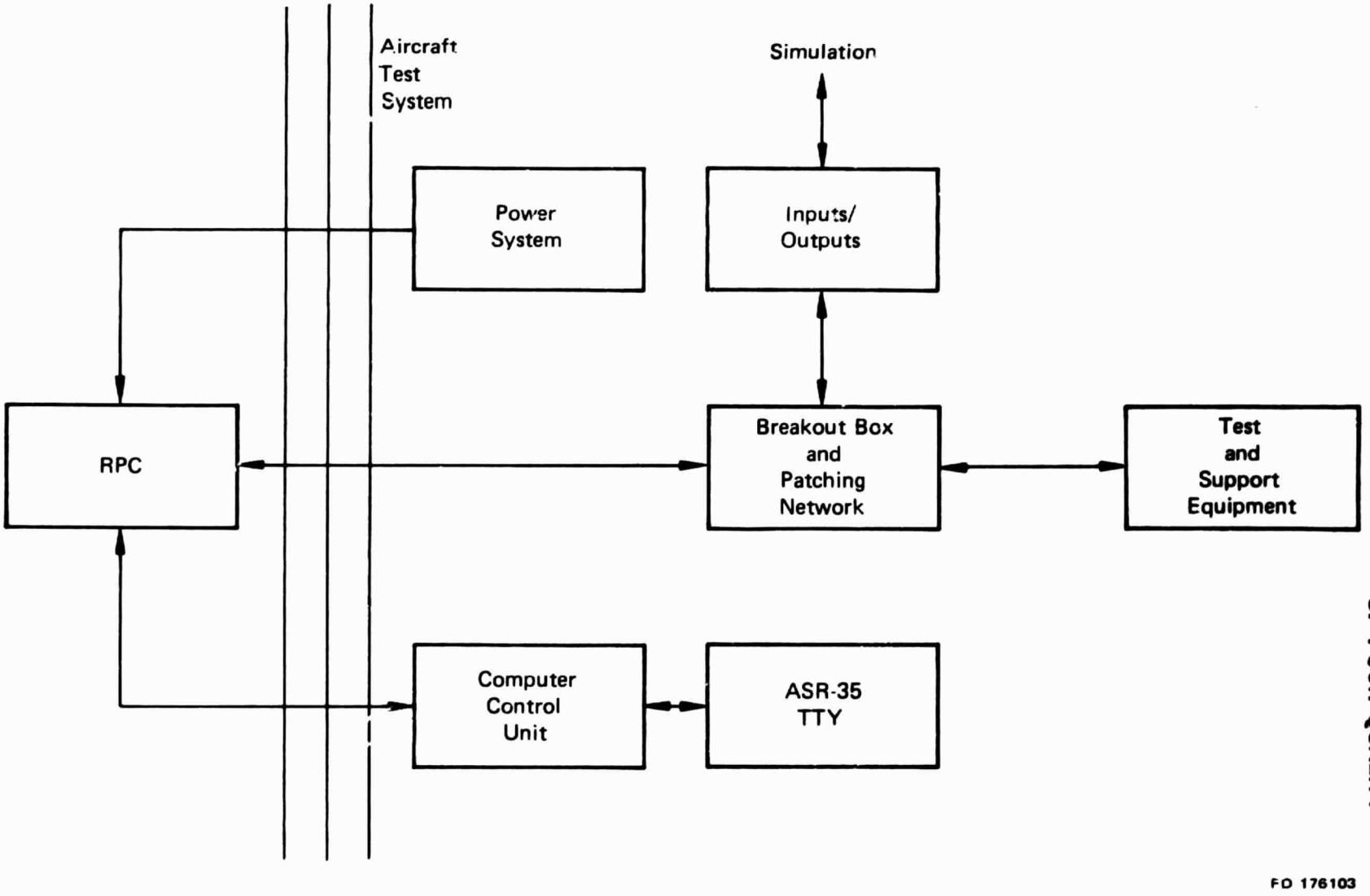

Figure IX-3. RPC Ground Support Equipment

3. Computer Control Unit (CCU)

The CCU is used for interface between the operator and the computer. With the CCU, the operator can manually load memory and observe various computer registers. The CCU interfaces with the computer and the ASR-35 Teletypewriter, high-speed paper-tape punch, and high-speed paper-tape reader.

D. GPD CONTROL SYSTEM DEVELOPMENT/INTEGRATION FACILITY

The GPD Control System Development/Integration Facility, also known as the Closed Loop Bench (CLB), is a state-of-the-art dedicated facility that supplements the control design/development process. Using system simulations specifically designed for use in the design/development cycle, the facility provides data normally acquired from expensive, difficult to schedule sea level and altitude tests, throughout the development cycle.

The facility supports all phases of the control development process "paper" design, engine model software development, implementation of control algorithm in digital controllers, data acquisition/reduction/presentation, and real-time/hardware-in-the-loop testing. A simplified representation of the facility configured for the F100 control system is shown in figure IX-4.

The hybrid computing equipment is schematically illustrated in figure IX-5. General peripheral equipment associated with the hybrid facility include a graphics terminal, AN terminal, plotter, printer, and mass storage.

A unique feature of the facility is the hybrid model's ability to "fly" the engine/airframe operational envelope in real time. Additional capabilities are as follows:

- Ability to use the simulation in a pure analytical design mode or coupled to control hardware for closed loop testing
- Ability to test either a single component, the total system, or a total system with the missing components replaced by computer simulation or emulations made from breadboard components
- Capability of testing the components or systems in an environment that can duplicate physical parameters that have an effect on the system's functional capability.

These facility capabilities will help ensure the integrated propulsion system configuration that has been selected for INTERACT with FADEC is the most cost effective approach meeting flight safety requirements.

Figure IX-4. Control System Development/Integration Facility

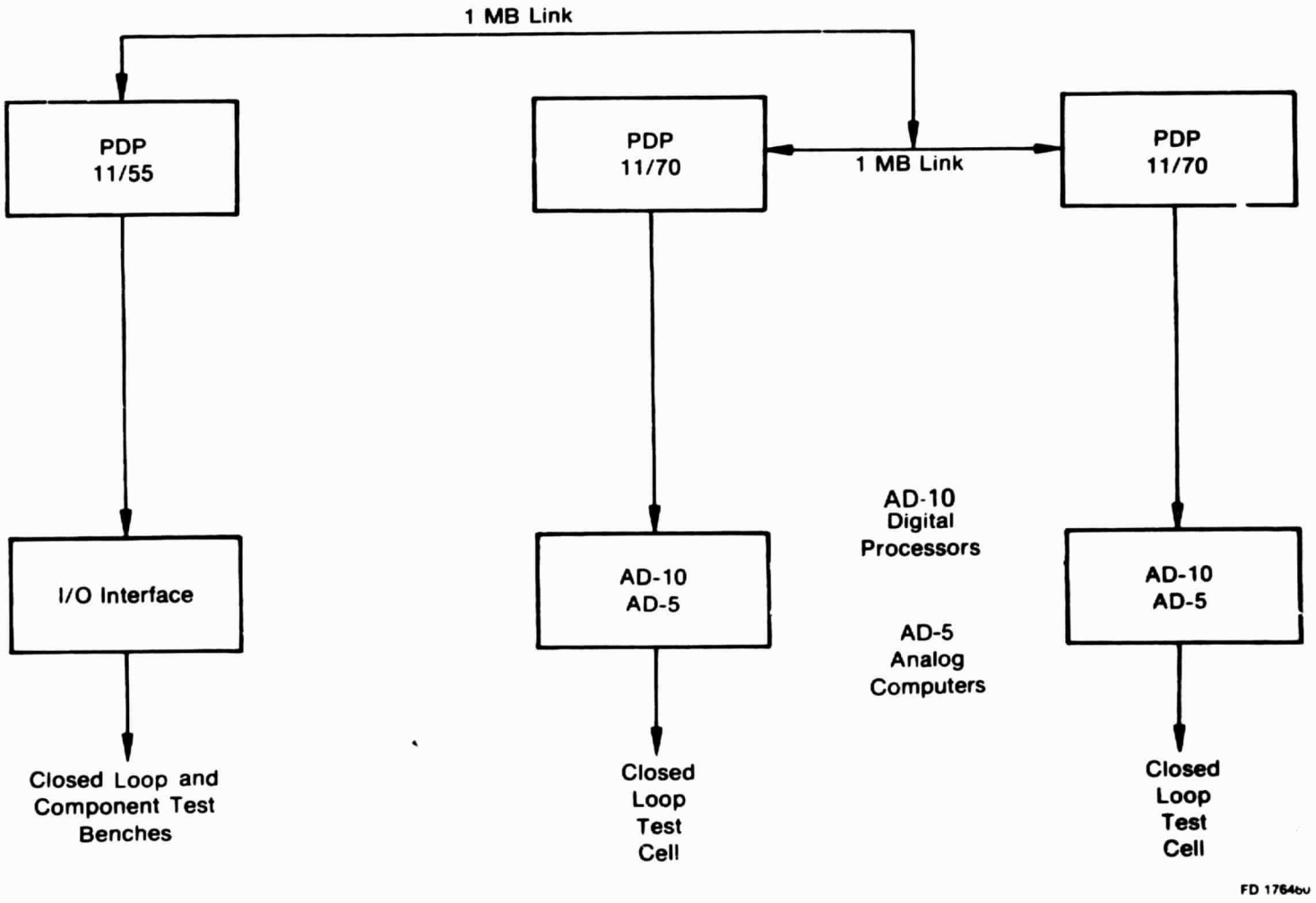

Figure IX-5. Control Development Facility Overview

SECTION X
APPLICABLE DOCUMENTS

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APPLICABLE DOCUMENTS

The following documents are applicable as references to the text of this report.

1. "Full Authority Digital Electronic Control, Phase I," Volumes I and II, Report FR-8652, dated June 1978, prepared under Contract N00019-76-C-0042.

2. "Propulsion/Flight Control Integration Technology (PROFIT) Design Analysis Status," NASA Contractor Report 144875, dated July 1978, prepared under Contract NAS4-2391.

3. "Interface Control Document for the Digital Propulsion Control Unit (Integrated Propulsion Control System), Revision G," Document Number D251-1006, dated January 1974, prepared under Contract F33615-73-C-2053.

4. "A Summary of the Digital Electronic Engine Control (DEEC) System," PWA Internal Document, dated 1978.

5. "YF100-PW-100 Training Handbook," PWA Internal Document, prepared by PWA Service School, dated 15 March 1972.

6. "Aircraft Internal Time Division Command/Response Multiplex Data Bus," Mil-Std-1553B, dated 21 Sept 1978.

7. "Electronic Air Inlet Controller Requirements," McDonnell Aircraft Company Procurement Specification PS68-870045, Rev. C